Single-Chip, Multiband 3G Femtocell Transceiver

ADF4602

FEATURES

- Single-chip multiband 3G transceiver
  - 3GPP 25.104 release 6 WCDMA/HSPA compatible
- UMTS band coverage
  - Local area Class BS in Band 1 to Band 6 and Band 8 to Band 10
- Direct conversion transmitter and receiver
- Minimal external components
  - Integrated multiband multimode monitoring
  - No Tx SAW or Rx interstage SAW filters
  - Integrated power management (3.1 V to 3.6 V supply)
  - Integrated synthesizers including PLL loop filters
  - Integrated PA bias control DACs/GPOs
- WCDMA and GSM receive baseband filter options
- Easy to use with minimal calibration
  - Automatic Rx DC offset control
  - Simple gain, frequency, mode programming
- Low supply current
  - 50 mA typical Rx current
  - 50 mA to 100 mA Tx current (varies with output power)
- 6 mm × 6 mm 40-pin LFCSP package

APPLICATIONS

- 3G home basestations (femtocells)
- 3G repeaters

FUNCTIONAL BLOCK DIAGRAM

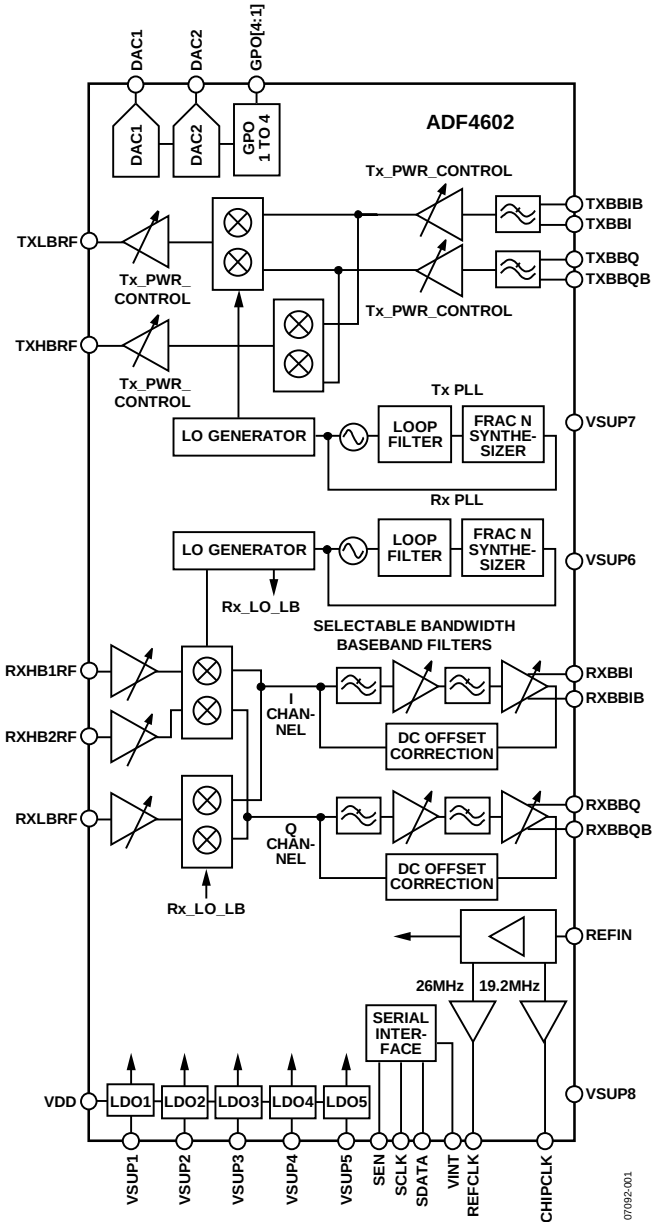

Figure 1.

Rev. 0

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REVISION HISTORY

10/09—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADF4602 is a 3G transceiver integrated circuit (IC) offering unparalleled integration and feature set. The IC is ideally suited to high performance 3G femtocells providing cellular fixed mobile converged (FMC) services. With only a handful of external components, a full multiband transceiver is implemented.

UMTS Band 1 through Band 6 and Band 8 through Band 10 are supported in a single device.

The receiver is based on a direct conversion architecture. This architecture is the ideal choice for highly integrated wideband CDMA (WCDMA) receivers, reducing the bill of materials by fully integrating all interstage filtering. The front end includes three high performance, single-ended low noise amplifiers (LNAs), allowing the device to support tri-band applications. The single-ended input structure eases interface and reduces the matching components required for small footprint single-ended duplexers. The excellent device linearity achieves good performance with a large range of SAW and ceramic filter duplexers.

The integrated receive baseband filters offer selectable bandwidth, enabling the device to receive both WCDMA and GSM-EDGE radio signals. The selectable bandwidth filter, coupled with the multiband LNA input structure, allows GSM-EDGE signals to be monitored as part of a UMTS home basestation.

The transmitter uses an innovative direct conversion modulator that achieves high modulation accuracy with exceptionally low noise, eliminating the need for external transmit SAW filters.

The fully integrated phase lock loops (PLLs) provide high performance and low power fractional-N frequency synthesis for both receive and transmit sections. Special precautions have been taken to provide the isolation demanded by frequency division duplex (FDD) systems. All VCO and loop filter components are fully integrated.

The ADF4602 also contains on-chip low dropout voltage regulators (LDOs) to deliver regulated supply voltages to the functions on chip, with an input voltage of between 3.1 V and 3.6 V.

The IC is controlled via a standard 3-wire serial interface with advanced internal features allowing simple software programming. Comprehensive power-down modes are included to minimize power consumption in normal use.

SPECIFICATIONS

V_{DD} = 3.1 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3.3 V and T_A = 25°C, 26 MHz reference input level = 0.7 V p-p.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
REFERENCE SECTION					
Reference Input					
Reference Input Frequency		26		MHz	
Reference Input Amplitude	0.1	0.7	2.0	V p-p	Single-ended operation, dc-coupled[1]
REFCLK Output (26 MHz)					
Output Load Capacitance		10	40	pF	
Output Swing		1.5		V p-p	10 pF load
Output Slew Rate		200		V/µs	10 pF load
Output Duty Cycle Variation		2		%	Input duty cycle = 50%
CHIPCLK Output (19.2 MHz)					
Output Load Capacitance		10	40	pF	
Frequency Multiplication Ratio	48/65		48/65	N/A	
Output Swing		1.5		V p-p	10 pF load
Output Duty Cycle Variation		2		%	Input duty cycle = 50%
Output Jitter		36		ps rms	
Lock Time		50		µs	
TRANSMIT SECTION					
I/Q Input					
Input Resistance		100		kΩ	Single-ended
Input Capacitance		2		pF	Single-ended
Differential Peak Input Voltage		500	550	mV pd	
Input Common-Mode Voltage	1.05	1.2	1.4	V	
Baseband Filter 3 dB Bandwidth		4.0		MHz	
TX Gain Control					
Maximum Gain		5		dB	1 V p-p differential baseband input
Gain Control Range		60		dB	
Gain Control Resolution		1/32		dB	Average of LSB steps
Gain Control Accuracy		1.0		dB	Any 1 dB step
		10		dB	Any 10 dB step
Gain Settling Time		1		µs	P_{OUT} within 0.1 dB of final value
RF Specifications (High Band)					
Carrier Frequency	1710		2170	MHz	
Output Impedance		50		Ω	
Output Power (P_{OUT})		−8		dBm	TM1 signal 64 DPCH
Output Noise Spectral Density		−155		dBc/Hz	40 MHz offset
		−161		dBc/Hz	80 MHz offset
		−161		dBc/Hz	95 MHz offset
		−163		dBc/Hz	190 MHz offset
Carrier Leakage		−35		dBc	P_{OUT} = −8 dBm
FDD EVM		5		%	P_{OUT} = −8 dBm
FDD ACLR		55		dB	±5 MHz, P_{OUT} = −8 dBm
		70		dB	±10 MHz, P_{OUT} = −8 dBm

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Specifications (Low Band)					
Carrier Frequency	824		960	MHz	
Output Impedance		50		Ω	
Output Power (P_{OUT})		−6		dBm	TM1 signal 64 DPCH
Output Noise Spectral Density		−158		dBc/Hz	45 MHz offset
Carrier Leakage		−35		dBc	P_{OUT} = −6 dBm
FDD EVM		5		%	P_{OUT} = −6 dBm
FDD ACLR		55		dB	±5 MHz, P_{OUT} = −6 dBm
		70		dB	±10 MHz, P_{OUT} = −6 dBm
RECEIVE SECTION					
Baseband I/Q Output					
Output Common Mode Voltage	1.15	1.2	1.35	V	Mode 1
	1.35	1.4	1.55	V	Mode 2
Differential Output Range		4		V p-p d	
Output DC Offset		±5		mV	WCDMA HPF mode
		±100		mV	GSM servo loop mode
Quadrature Gain Error		0.3	0.7	dB	
Quadrature Phase Error		1		°rms	
In-Band Gain Ripple		0.2		dB	
Low-Pass Filter Rejection					
WCDMA (Seventh Order)		30		dB	@2.7 MHz
		45		dB	@3.5 MHz
		84		dB	@5.9 MHz
		110		dB	@10 MHz
WCDMA (Fifth Order)		14		dB	@2.7 MHz
		31		dB	@3.5 MHz
		55		dB	@5.9 MHz
		80		dB	@10 MHz
GSM		12		dB	@200 kHz
		47		dB	@400 kHz
		90		dB	@800 kHz
Differential Group Delay					
WCDMA		250		ns	1.92 MHz band
GSM		200		ns	100 kHz band
Receiver Gain Control					
Maximum Voltage Gain		102		dB	WCDMA mode
Gain Control Range		90		dB	
Gain Control Resolution		1		dB	
Gain Control Step Error		±1		dB	1 dB step
		±2		dB	10 dB step
RF Specifications (High Band)					
Input Frequency	1710		2170	MHz	
Input Impedance		50		Ω	
Input Return Loss		−20		dB	
Noise Figure		4.0		dB	TX power of −8 dBm, spur-free measurement[2]
Maximum Input Power[3]			−20	dBm	Maximum LNA gain
			−2	dBm	Minimum LNA gain
Input IP3		−7		dBm	±10 MHz and ±20 MHz Offset, 59 dB gain
		0			85 MHz and 190 MHz Offset, 59 dB gain
Input IP2		53		dBm	80 MHz offset
		65		dBm	190 MHz offset
EVM		8		%	−60 dBm input

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Specifications (Low Band)					
Input Frequency	824		960	MHz	
Input Impedance		50		Ω	
Input Return Loss		−20		dB	
Noise Figure		4.0		dB	80 dB gain, TX power of −8 dBm
Maximum Input Power[3]			−20	dBm	Maximum LNA gain
			−2	dBm	Minimum LNA gain
Input IP3		2		dBm	±10 MHz and ±20 MHz offset, 59 dB gain
		5		dBm	45 MHz and 90 MHz offset, 59 dB gain
Input IP2		40		dBm	45 MHz offset
EVM		7		%	−60 dBm input
Synthesizer Section					
Channel Resolution		50		kHz	
Lock Time[3]			200	µs	
DAC/GPO CONTROL					
DAC1					
Resolution		5		bits	
Output Range	2.3		3.15	V	V_{DD} > 3.15 V
Absolute Accuracy		±50		mV	Any code, V_{DD} > 3.2 V
Output LSB Step		25		mV	
Output Capacitive Load			1	nF	
Output Current	−10		+10	mA	
Output Impedance		1		Ω	
DAC2					
Resolution		6		bits	
Output Range	0		2.85	V	
DNL		±0.5		LSB	No load
INL		±1.0		LSB	No load
Output Capacitive Load			1	nF	
Output Current	−5		+5	mA	
Output Impedance		5		Ω	
GPO1 to GPO4					
Output Current			2	mA	GPO1, GPO2, GPO3
			10	mA	GPO4
Output High Voltage	2.6			V	Maximum output current
Output Low Voltage			0.2	V	Maximum output current
Switching Time		1		µs	5 pF load
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.2		2.1	V	1.8 V readback mode[4]
Input High Voltage, V_{INH}	1.2		3.3	V	2.8 V readback mode[4]
Input Low Voltage, V_{INL}			0.6	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS (SDATA)					
Output High Voltage, V_{OH}	V_X − 0.45			V	V_X = VINT or VSUP8, I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.45	V	I_{OL} = 500 µA
CLK_{OUT} Rise/Fall			5	ns	
CLK_{OUT} Load			10	pF	
TEMPERATURE RANGE (T_A)	0		85	°C	

Parameter	Min	Typ	Max	Unit	Test Conditions
POWER SUPPLIES					
Voltage Supply					
VDD	3.1	3.3	3.6	V	Main supply input
VSUP1		2.6		V	Output from internal LDO1, 10 mA rating, supply for RX VCO
VSUP2		2.8		V	Output from Internal LDO2, 30 mA rating, supply for RX baseband and RX down-converter
VSUP3		1.9		V	Output from internal LDO3, 10 mA rating, supply for RX LNAs
VSUP4		2.6		V	Output from internal LDO4, 10 mA rating, supply for TX VCO
VSUP5		2.8		V	Output from internal LDO5, 100 mA rating, supply for TX modulator, TX baseband, PA control DACs
VSUP6		1.9		V	Supply input for RX synthesizer, connect to VSUP3
VSUP7		1.9		V	Supply input for TX synthesizer, connect to VSUP3
VSUP8		2.8		V	Supply input for reference section, connect to VSUP2
VINT	1.6	1.8	2.0	V	Supply input for serial interface control logic
CURRENT CONSUMPTION					
Transmit Current Consumption					V_{DD} = 3.6 V, output is matched into 50 Ω
−8 dBm Output Level		100		mA	F_{RF} = 2170 MHz
−28 dBm Output Level		50		mA	F_{RF} = 2170 MHz
Receive Current Consumption		50		mA	

[1] The reference frequency should be dc coupled to the REFIN pin. It is ac-coupled internally.
[2] The noise figure measurement does not include spurious due to harmonics of the 26 MHz reference frequency. Spurs appear at integer multiples of the reference frequency (every 26 MHz), degrading the receive sensitivity by about 6 dB.
[3] Guaranteed by design, not production tested.
[4] Bit sif_vsup8 in Register 2 controls whether 1.8 V readback mode or 2.8 V readback mode is selected. See the Serial Port Interface (SPI) section for more details.

TIMING CHARACTERISTICS

V_{DD} = 3.1 V to 3.6 V, VGND = 0 V, T_A = 25°C, unless otherwise noted. Guaranteed by design but not production tested.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	62	ns min	SEN high to write time
t_2	10	ns min	SEN to SCLK setup time
t_3	10	ns min	SDATA to SCLK setup time
t_4	10	ns min	SDATA to SCLK hold time
t_5	31	ns min	SCLK high duration
t_6	31	ns min	SCLK low duration
t_7	10	ns min	SEN to SCLK hold time
t_8	20	ns max	SEN to SDATA valid delay
t_9	20	ns max	SCLK to SDATA valid delay
t_{10}	20	ns max	SEN to SDATA disabled delay

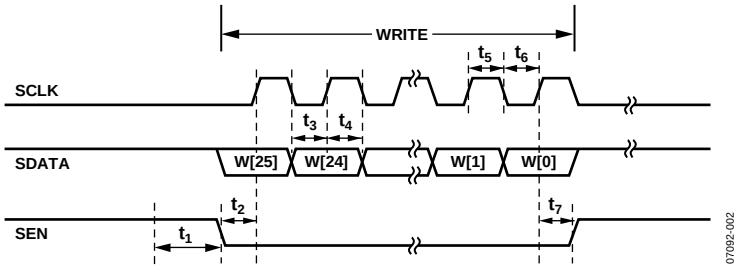

Figure 2. Serial Interface Write Diagram

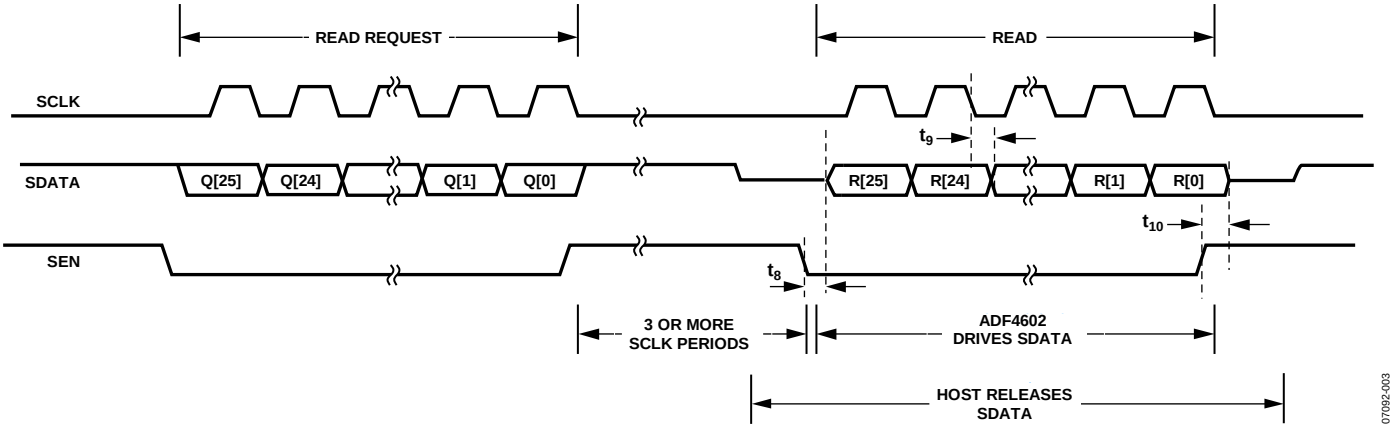

Figure 3. Serial Interface Read/Write Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to GND	−0.3 V to +4 V
VSUP1, VSUP2 to GND	−0.3 V to +3.6 V
VSUP4, VSUP5, VSUP6, VSUP7, VSUP8, VSUP9 to GND	−0.3 V to +3.6 V
VSUP3 to GND	−0.3 V to +2.0 V
VINT to GND	−0.3 V to +2.0 V
Analog I/O Voltage to GND	−0.3 V to VDD + 0.3 V
Digital I/O Voltage to GND	−0.3 V to VDD + 0.3 V
Operating Temperature Range	
Commercial (B Version)	0°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance	32°C/W
Reflow Soldering	
Peak Temperature	240°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

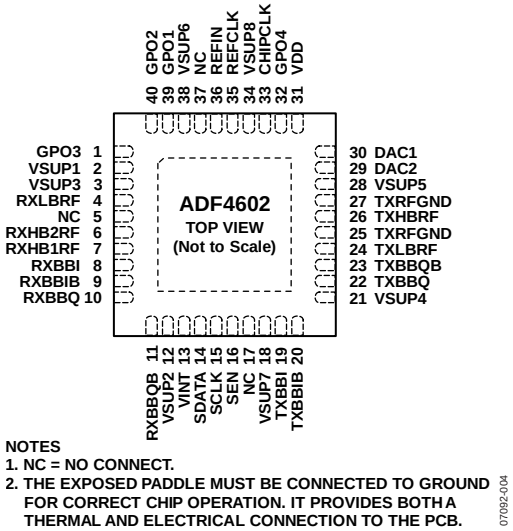

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	GPO3	General Purpose Output 3. Digital output. This is used for external switch or PA control.
2	VSUP1[1]	Output from LDO 1. Supply for receive VCO. Nominal value of 2.6 V. 100 nF decoupling to ground is required.
3	VSUP3[1]	Output from LDO 3. Supply for receive LNA. Nominal value of 1.9 V. 100 nF decoupling to ground is required.
4	RXLBRF	Receive Low Band LNA Input.
5	NC	No Connect. Do not connect to this pin.
6	RXHB2RF	Receive Second High Band LNA Input. Should be used for Band 2.
7	RXHB1RF	Receive First High Band LNA Input. Should be used for Band 1.
8	RXBBI	Receive Baseband I Output.
9	RXBBIB	Complementary Receive Baseband I Output.
10	RXBBQ	Receive Baseband Q Output.
11	RXBBQB	Complementary Receive Baseband Q Output.
12	VSUP2[1]	Output from LDO 2. Supply for receive downconverter and baseband. Nominal value of 2.8 V. 100 nF decoupling to ground is required.
13	VINT	Serial Port Supply Input. 1.8 V should be applied to this pin.
14	SDATA	Serial Port Data Pin. This can be an input or output.
15	SCLK	Serial Clock Input.
16	SEN	Serial Port Enable Input.
17	NC	No Connect. Do not connect to this pin.
18	VSUP7[1]	Transmit Synthesizer Supply Input. Connect to VSUP3 and decouple with 100 nF to ground.
19	TXBBI	Transmit Baseband I Input.
20	TXBBIB	Complementary TX Baseband I Input.
21	VSUP4[1]	Output from LDO4. Supply for transmit VCO. Nominal value of 2.8 V. 100 nF decoupling to GND is required.
22	TXBBQ	Transmit Baseband Q Input.
23	TXBBQB	Complementary TX Baseband Q Input.
24	TXLBRF	Low Band Transmit RF Output. This can output in the range of 824 MHz to 960 MHz.
25	TXRFGND	Transmit RF Ground. Connect this pin to ground.
26	TXHBRF	High Band Transmit RF Output. This can output in the range of 1710 MHz to 2170 MHz.
27	TXRFGND	Transmit RF Ground. Connect this pin to ground.
28	VSUP5[1]	Output from LDO 5. Supply for transmit modulator, baseband, power detector, and DACs. Nominal value of 2.8 V. 100 nF decoupling to ground is required.
29	DAC2	Output from DAC2.
30	DAC1	Output from DAC1.

Pin No.	Mnemonic	Function
31	VDD	Main Supply Input.
32	GPO4	Digital Output. This is used for switch or PA control.
33	CHIPCLK	Chip Clock Output.
34	VSUP8[1]	Reference Clock Supply Input. Connect to VSUP2, and decouple to ground with 100 nF.
35	REFCLK	Reference Clock Output.
36	REFIN	Reference Clock Input. The reference is ac-coupled internally.
37	NC	No Connect. Do not connect to this pin.
38	VSUP6[1]	Receive Synthesizer Supply Input. Connect to VSUP3 and decouple to ground with 100 nF.
39	GPO1	Digital Output. This is used for switch or PA control.
40	GPO2	Digital Output. This is used for switch or PA control.
	EPAD	Exposed Paddle Under Chip. This must be connected to ground for correct chip operation. It provides both a thermal and electrical connection to the PCB.

[1]Y5V capacitors are not recommended for use with these pins. X7R, X5R, C0G or a similar type of capacitor should be used.

TYPICAL PERFORMANCE CHARACTERISTICS

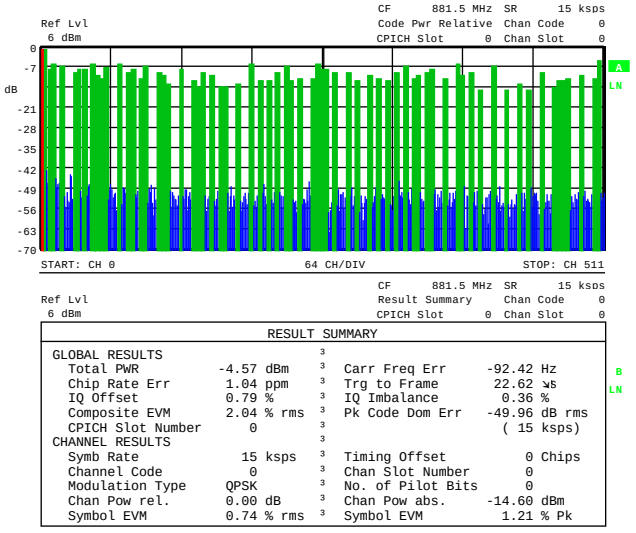

Figure 5. UMTS Band 5 Transmit EVM, Test Model 1, 64 DPCH, 2% EVM

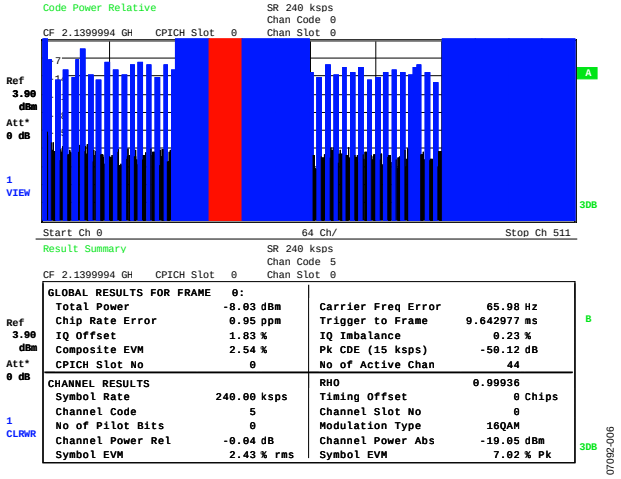

Figure 6. UMTS Band 1 Transmit EVM, Test Model 5, 2.5% EVM

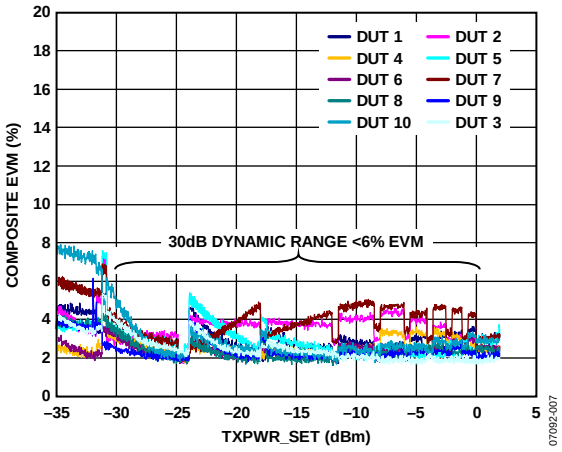

Figure 7.Transmit EVM vs. TXPWR_SET (dBm), Measured Across 10 DUTS, Four Calibration Points Applied

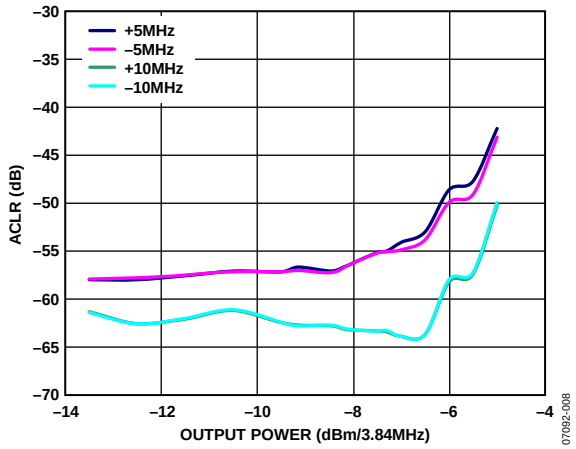

Figure 8. TXHBRF Transmit ACLR vs. Output Power, Test Model 1 Signal, 10.54 dB PAR, 217 MHz

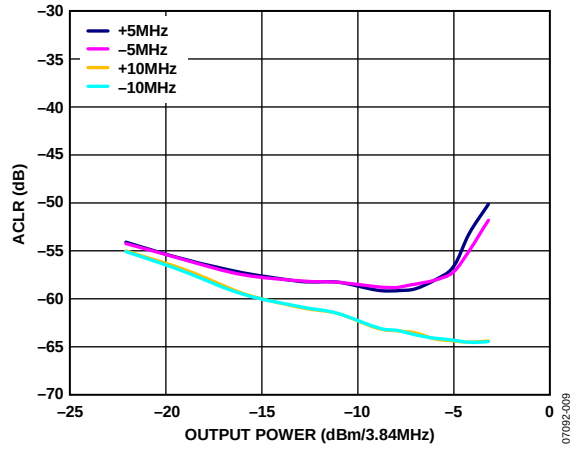

Figure 9. TXLBRF Transmit ACLR vs. Output Power, Test Model 1 Signal, 10.54 dB PAR, 881 MHz

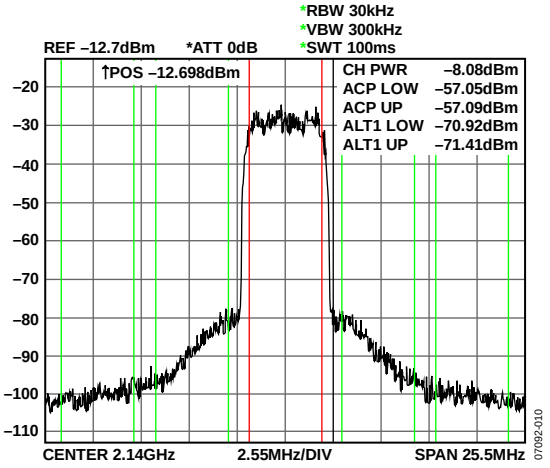

Figure 10. TXHBR Transmit ACLR, 2140 MHz

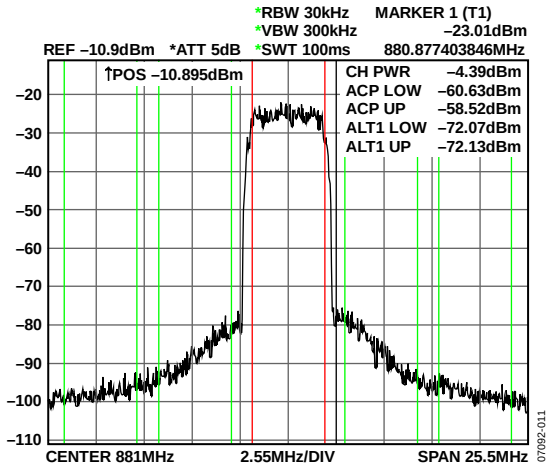

Figure 11. TXLBRF Transmit ACLR, 881 MHz

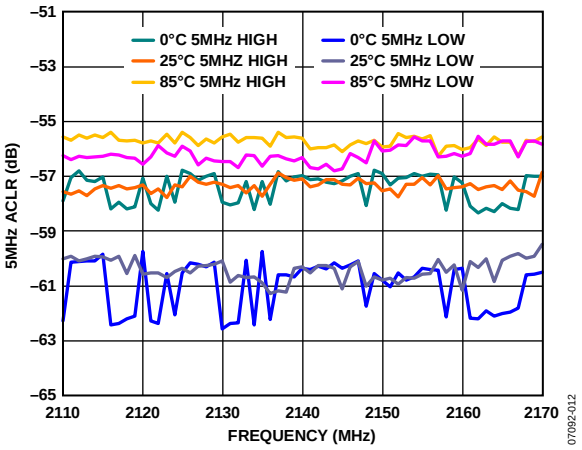

Figure 12. Transmit ACLR vs. Frequency and Temperature (Band 1), Transmit Output Power = –8 dBm

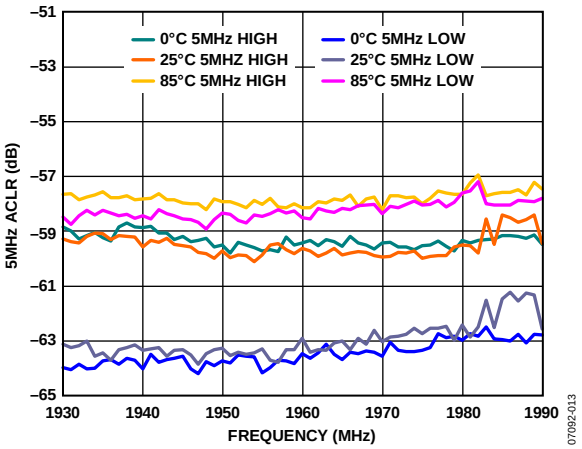

Figure 13. Transmit ACLR vs. Frequency and Temperature (Band 2), Transmit Output Power = –8 dBm

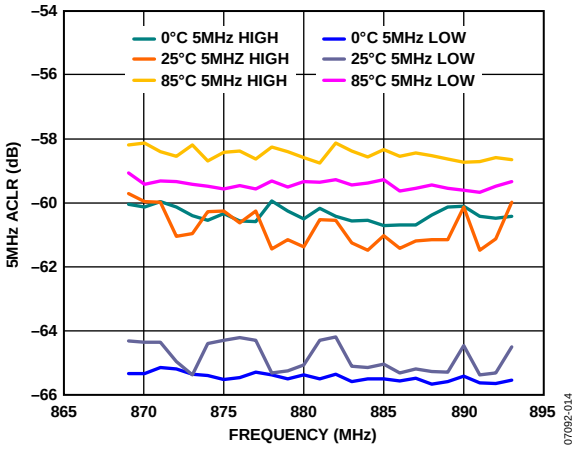

Figure 14. Transmit ACLR vs. Frequency and Temperature (Band 5), Transmit Output Power = –7 dBm

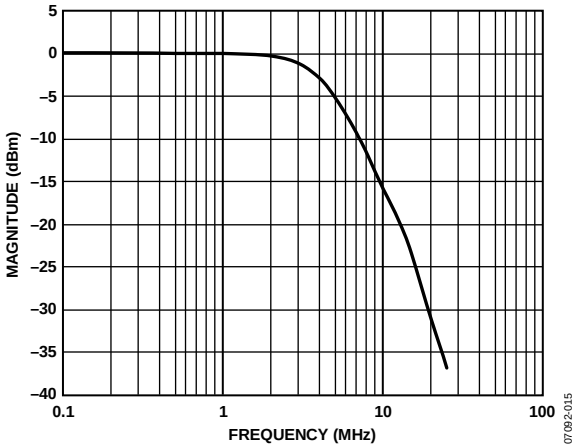

Figure 15. Transmit Baseband Filter Response

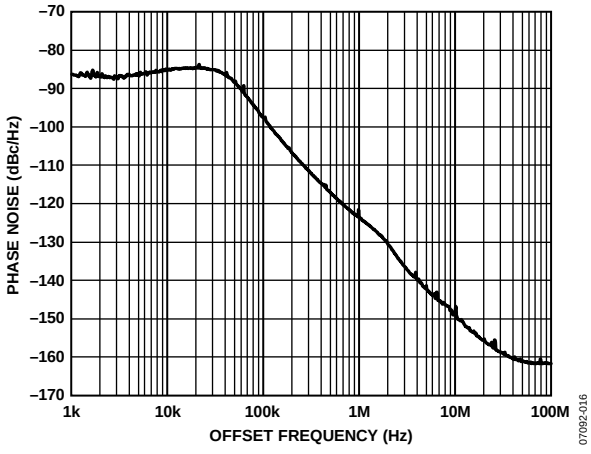

Figure 16. Transmit Synthesizer Phase Noise

Figure 17. Current Consumption vs. Transmit Output Power; Frequency = 2170 MHz, V_{DD} = 3.3 V, Test Model 5 Signal, Receiver Disabled

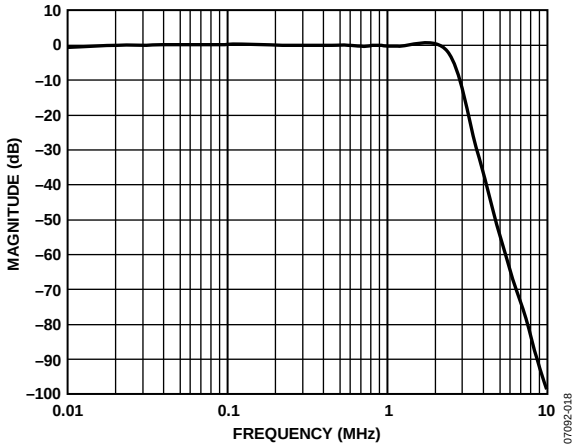

Figure 18. Receive WCDMA Baseband Filter Response

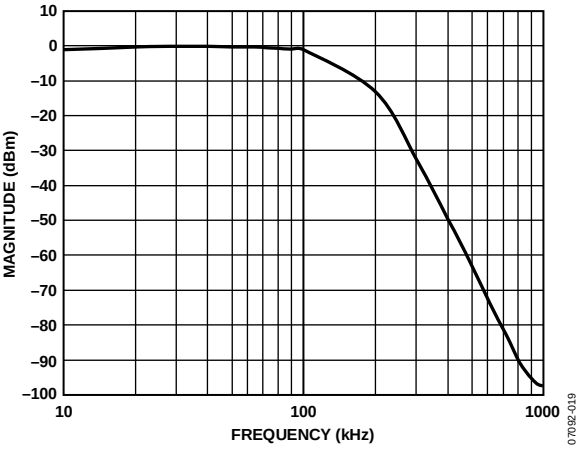

Figure 19. Receive GSM Baseband Filter Response

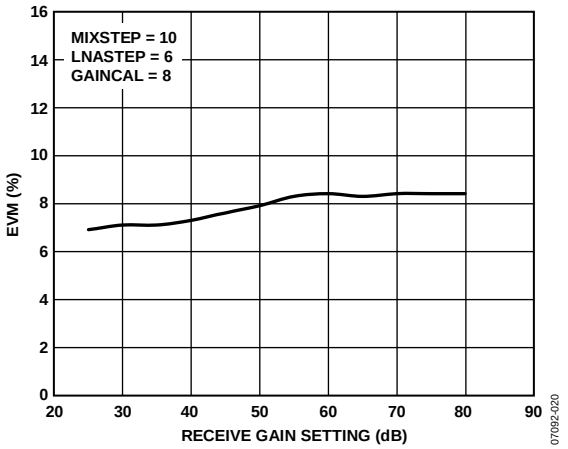

Figure 20. Receive EVM vs. Gain; 2.84 MHz QPSK Modulated Input Signal, WCDMA Receive Baseband Filter

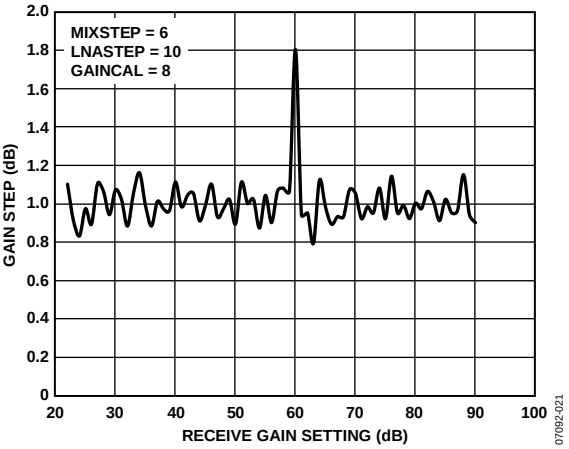

Figure 21. Receive Gain Step Error vs. Gain Setting, 1 dB Steps, Measurement was taken by injecting known signal level and measuring the gain through the device. The gain was then stepped through all settings in 1 dB steps, and the gain step change measured in each case.

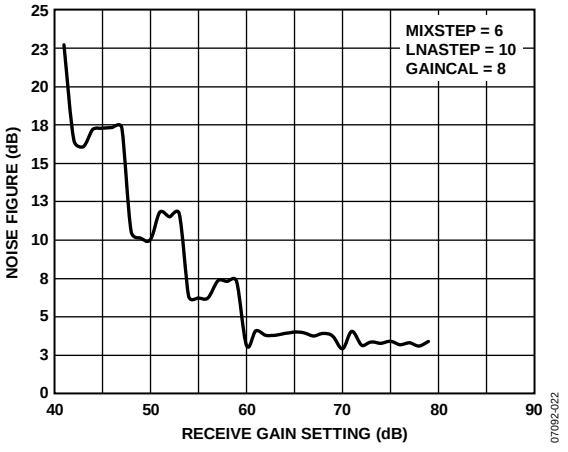

Figure 22. Receiver Noise Figure vs. Gain. Rx Frequency = 1955 MHz

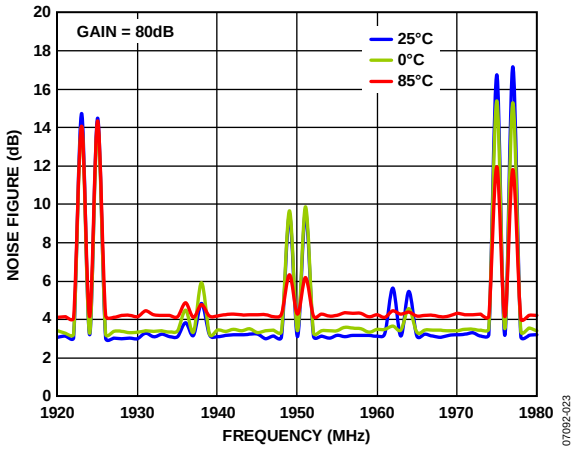

Figure 23. HB1 Receive Noise Figure vs. Frequency

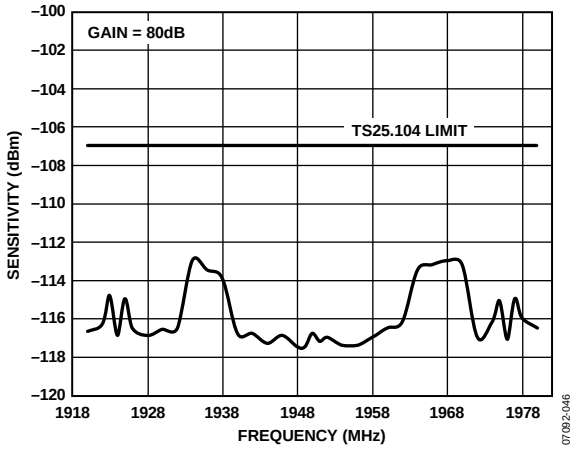

Figure 26. Receive Sensitivity vs. Frequency (See the Receive Sensitivity Section for More Details)

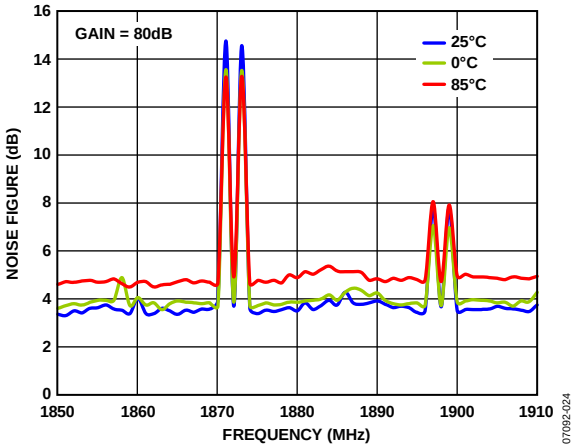

Figure 24. HB2 Receive Noise Figure vs. Frequency

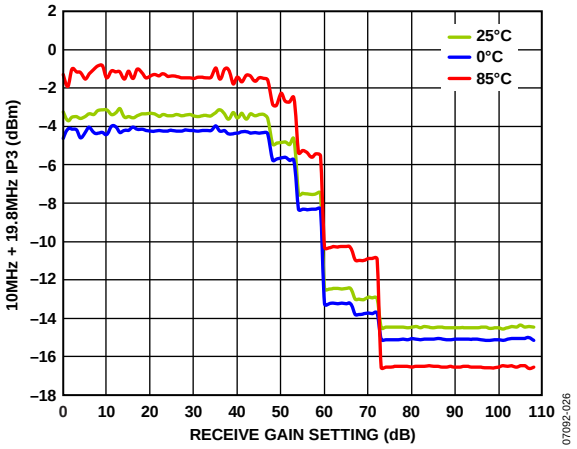

Figure 27. HB1 Receive IP3, 10 MHz + 19.8 MHz vs. Gain Setting

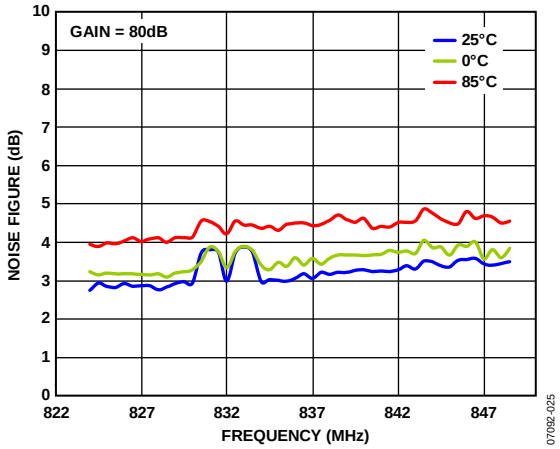

Figure 25. LB Receive Noise Figure vs. Frequency

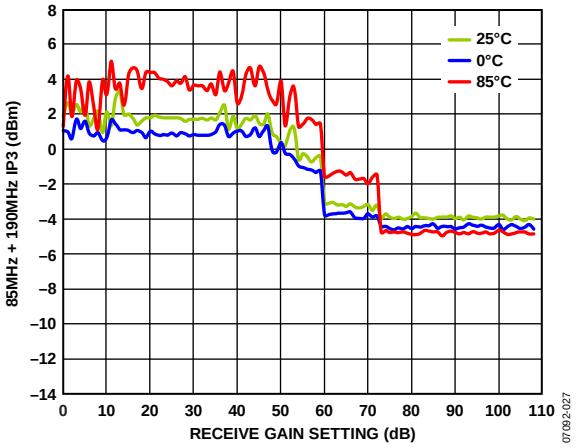

Figure 28. HB1 Receive IP3, 85 MHz + 190 MHz vs. Gain Setting

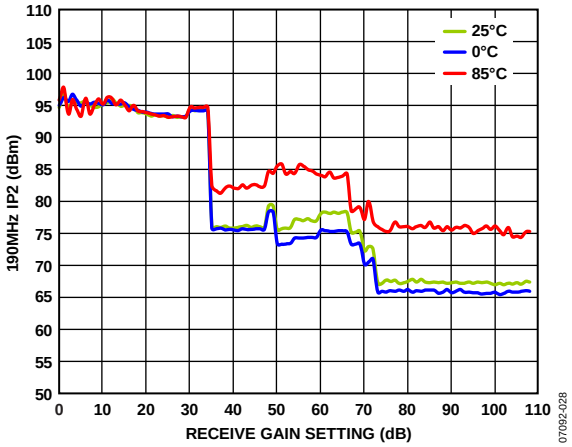

Figure 29. HB1 Receive IP2, 190 MHz vs. Gain Setting

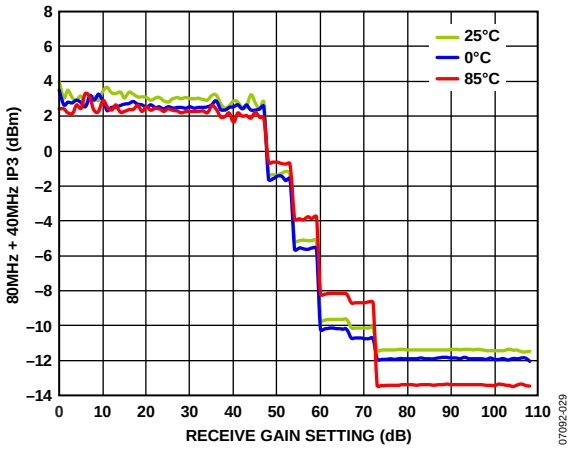

Figure 30. HB2 Receive IP3, 80 MHz + 40 MHz vs. Gain Setting

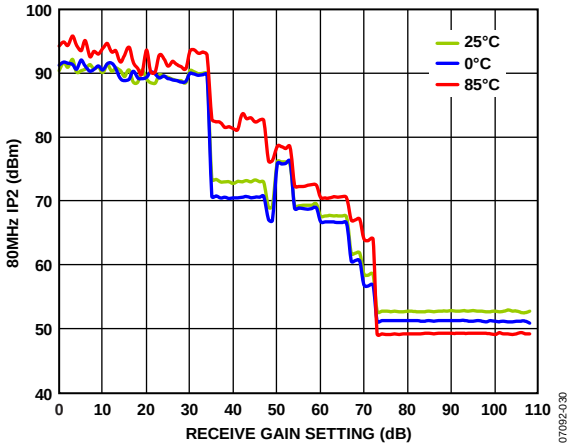

Figure 31. HB2 Receive IP2, 80 MHz vs. Gain Setting

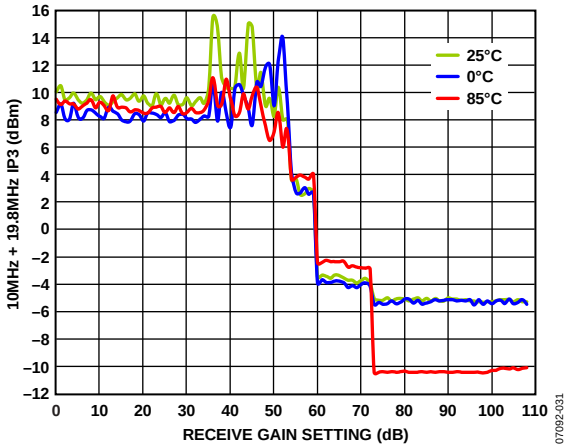

Figure 32. LB Receive IP3, 10 MHz + 19.8 MHz vs. Gain Setting

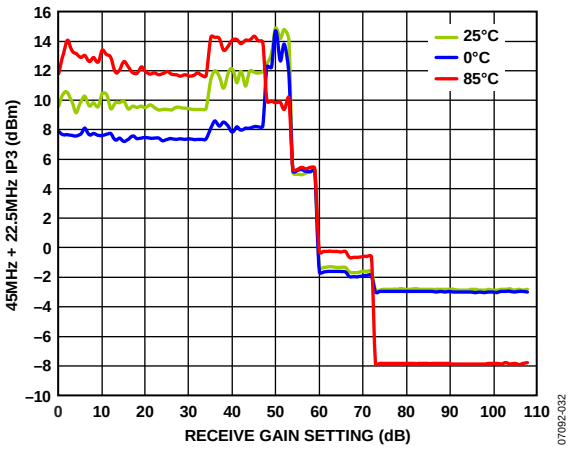

Figure 33. LB Receive IP3, 45 MHz + 22.5 MHz vs. Gain Setting

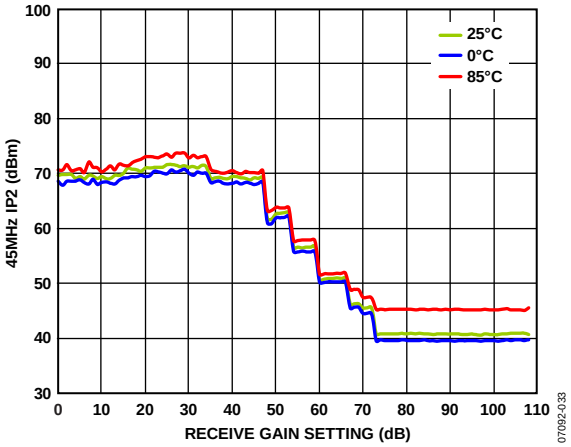

Figure 34. LB Receive IP2, 45 MHz vs. Gain Setting

THEORY OF OPERATION

TRANSMITTER DESCRIPTION

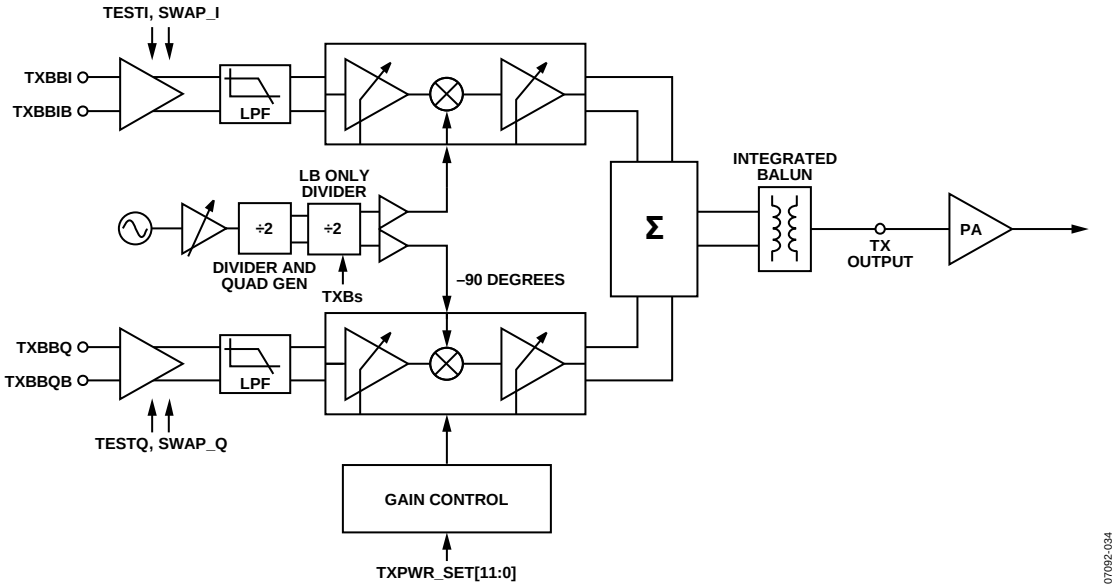

Figure 35. Transmitter Block Diagram

The ADF4602 contains a highly innovative low noise variable gain direct conversion transmitter architecture, that removes the need for external transmit SAW filters. The direct conversion architecture significantly reduces the risk of transmit harmonics across all bands due to the simplified nature of the frequency plan. See Figure 35 for a block diagram.

I/Q Baseband

The baseband interface for the I and Q channels is a differential, dc-coupled input, supporting a wide range of input common-mode voltages (V_{CM}). The allowable input common-mode range is 1.05 V to 1.4 V. The maximum signal swing allowed is 550 mV peak differential. This corresponds to a 1.1 V peak-to-peak differential on either the I or Q channel. Figure 36 shows a graphical definition of peak differential voltage and V_{CM}.

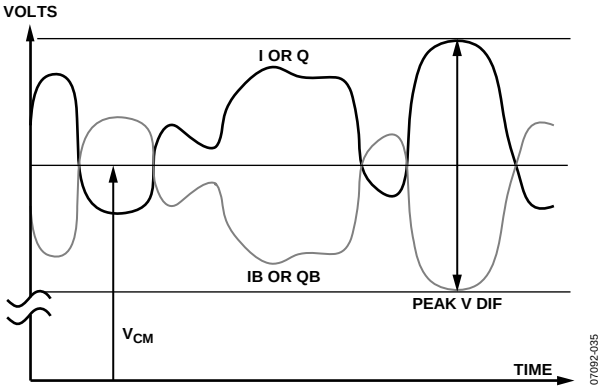

Figure 36. Transmit Baseband Input Signals

The baseband input signals pass through a second order Butterworth filter prior to the quadrature modulator. The cutoff frequency is 4 MHz. This gives some rejection of the DAC images. The filter also helps to suppress any spurious signals that might be coupled to the baseband terminals on the PCB.

For ease of PCB routing between the ADF4602 and the transmit DAC, the I and Q differential inputs can be internally swapped. For user test purposes, the I and Q inputs can also be internally shorted together and a dc offset applied. This produces a large carrier at the RF output, which is useful for signal path integrity testing.

I/Q Modulator

The I/Q modulator converts the transmit baseband input signals to RF. Calibration techniques are used to maintain accurate IQ balance and phase across frequency and environmental conditions, thus ensuring that 3GPP carrier leakage and EVM and ACLR requirements are met with good margin under all conditions. The on-chip calibrations are carried out during the transmit PLL lock time specified and are self-contained, requiring no additional input from the user.

The modulator has an 80 dB gain control range, programmable in 1/32 of a decibel step. The 12-bit word txpwr_set[11:0] in Register 28 controls the transmit output power. The setting is referenced to a full-scale (500 mV peak differential) sine wave signal applied to the transmit baseband inputs. To calculate the output power when a WCDMA modulated signal with a certain peak-to-average ratio is applied, Equation 1 should be used.

$$Output\ Power\ (dBm/3.84\ MHz) = txpwr(\text{dBm}) - PAR(\text{dB}) \quad (1)$$

where *txpwr*(dBm) is the txpwr_set[11:0] value converted to dBm, and *PAR* is the peak-to-average ratio of the WCDMA signal. For example, if an output power of −8 dBm is required for a WCDMA signal with a peak-to-average ratio of 10 dB

$$txpwr(\text{dBm}) = -8\ \text{dBm} + 10\ \text{dB} = +2\ \text{dBm}$$

The current consumption of the modulator scales with output power. When the TX power is backed off from maximum, the transceiver benefits from lower power dissipation.

VCO Output

The TX VCO output is fed to a tuned buffer stage and then to the quadrature generation circuitry. The tuned buffer ensures that minimum current and LO related noise is generated in the VCO transport. This action is transparent to the user. The quadrature generator creates the highly accurate phased signals required to drive the modulator and also acts as a divide-by-2. In low band, an additional divide-by-2 is used in the VCO transport path, which is bypassed in high band. This is done to minimize the VCO tuning range required to cover all the bands.

The phase accuracy of the signals is important in ensuring good modulation quality and accurate output power. An on-chip calibration ensures that the phased signals are exactly 90° out of phase. This calibration runs each time the frequency is changed or if the txpwr_set[11:0] word is written to. If the temperature of the device changes, this calibration should be updated. To run the calibration, the user should simply write to the txpwr_set[11:0] word for each five degree change in temperature, or update the value regularly (every few seconds) between WCDMA frames or timeslots. This ensures that good EVM and accurate output power are maintained as the temperature of the device changes.

TX Output Baluns

The baseband input, modulator, and all associated circuitry are fully differential to maintain high signal integrity and noise immunity. However, a differential output is not optimal for the user because most power amplifiers (PAs) are singled-ended. This situation would normally require additional external matching components or a differential to single-ended SAW filter structure. With the ADF4602, the SAW filter is not necessary, and the required low loss balun is fully integrated, converting the differential internal signals to a single-ended 50 Ω output, thus allowing easy interfacing to the PA.

The high band output is available at the TXHBRF pin, and the low band output is available at the TXLBRF pin. These are directly connected to a 50 Ω load, if necessary, and do not require ac-coupling.

DACS

The ADF4602 integrates two DACs that are designed to interface to an external PA to control reference or bias nodes within the PA. If this function is not required, the DACs are used for any general purpose or powered down if not required.

DAC1 is a 5-bit voltage output DAC. The output range is from 2.3 V to 3.15 V (for V_{DD} > 3.15 V). The DAC1 output stage is supplied directly from VDD, with the capability to supply 10 mA of current to within 50 mV of V_{DD}. For high accuracy, the DAC reference is supplied from LDO5, which is internally trimmed to 25 mV accuracy. The DAC1 output is set by the PADAC1[4:0] word.

DAC2 is a 6-bit voltage output DAC with a range from 0 V to 2.8 V. LDO5 supplies both the reference voltage and full-scale output voltage for DAC2. The output voltage is set by the padac2_ow[5:0] word. The dacgpo_owen bit must also be set high if control of DAC2 is required.

Both DACS are powered down by writing the code, 0x0, to the respective control register.

GENERAL PURPOSE OUTPUTS

Four general-purpose outputs (GPOs) are provided on the ADF4602. These are used to control PA bias modes or, more commonly, the GPOs are used to control external RF front-end switches in the transmit/receive path. The GPOs are simple 3 V digital output drivers. GPO1 to GPO3 are capable of supplying a maximum current of 2 mA, whereas GPO4 can supply up to 10 mA.

For operation of the GPOs, Bit dacgpo_owen must be set to 1. The GPOs are then controlled via the gpo_ow[3:0] word.

RECEIVER DESCRIPTION

The ADF4602 contains a fully integrated direct conversion receiver designed for multiband WCDMA femtocell applications. High performance, low power consumption, and minimal external components are the key features of the design. Figure 37 shows a block diagram of the receiver, which consists of three LNA blocks for multiband operation, high linearity I/Q mixers, advanced baseband channel filtering, and a DC offset compensation circuit.

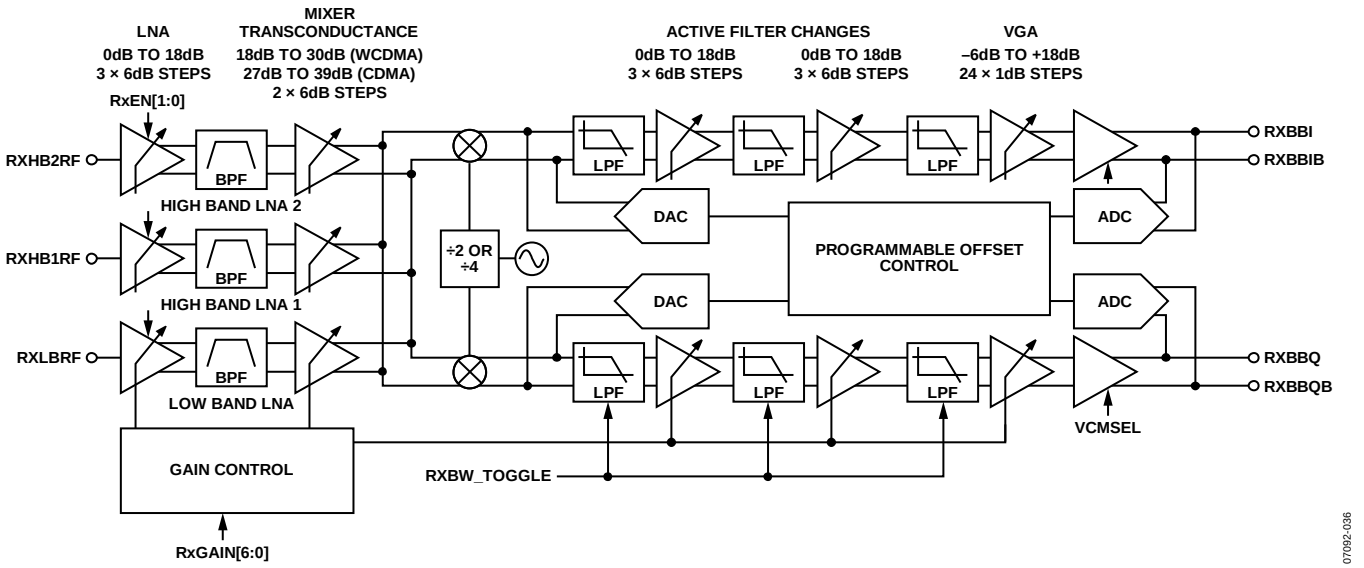

Figure 37. Receiver Block Diagram

LNAs

The ADF4602 contains three tunable RF front ends suitable for all major 3GPP frequency bands. Two are suitable for high band operation in the region 1700 MHz to 2170 MHz. One is suitable for operation from 824 MHz to 960 MHz. Thus, the three integrated LNAs offer the designer the opportunity to create multiband and regional specific variants with no additional components.

LNA power control and internal band switching is fully controlled by the serial interface.

The ADF4602 LNAs are designed for 50 Ω single-ended inputs, thus further simplifying the front-end design and providing easy matching with minimal components. Typically, a two-component match is required: a series and shunt inductor. Within the LNA, the signal is converted to a differential path for signal processing in subsequent blocks within the receive signal chain.

Interstage RF filtering is fully integrated, ensuring that external out-of-band blockers are suitably attenuated prior to the mixer stages. The LNA characteristic is designed to provide additional filtering at the transmitter frequency offset.

The LNAs are enabled by programming bits rxbs[1:0] in Register 1. LNA input HB1 should be used for UMTS Band 1 operation, and HB2 should be used for UMTS Band 2 operation.

Mixers

High linearity quadrature mixer circuits are used to convert the RF signal to baseband in-phase and quadrature components. Although not shown in Figure 37, two mixer sections exist: one optimized for the high band LNA outputs and one optimized for the low band. The high band and low band mixer outputs are combined and then driven directly into the first stage of the baseband low-pass filter, which also acts to reduce the level of the largest blocking signals, prior to baseband amplification.

Quadrature drive is provided to the mixers from the receiver synthesizer section by the VCO transport system, which includes a programmable divider, so that the same VCO is used for both high and low bands. Excellent 90° quadrature phase and amplitude match are achieved by careful design and layout of the mixers and VCO transport circuits.

Baseband Section

The ADF4602 baseband section is a distributed gain and filter function designed to provide a maximum of 54 dB gain with 60 dB gain control range. Through careful design, pass band ripple, group delay, signal loss, and power consumption are kept to a minimum. Filter calibration is performed during the manufacturing process, resulting in a high degree of accuracy and ease of use.

Three baseband filters are available on the ADF4602, as shown in Table 5. Bits rxbw_toggle[2:0] are used to select the mode of operation. The seventh order WCDMA filter with 1.92 MHz cutoff ensures that good attenuation of the adjacent channel should be used to meet blocking/adjacent channel selection specifications in femtocell applications. The GSM filter has a 100 kHz cut-off and is intended for use as a monitoring receiver in a home base station. The fifth order WCDMA filter provides less attenuation of the adjacent channel, so it should not be used in femtocell applications.

The I and Q channels can be internally swapped, thus allowing optimum PCB routing between radio and analog baseband. This is achieved using the swapi and swapq bits.

Table 5. Receive Baseband Filter Modes

Mode	Filter Cutoff Frequency (f_C)
Seventh Order WCDMA	1.92 MHz
Fifth Order WCDMA	1.92 MHz
GSM	100 kHz

The receive baseband outputs have a programmable common mode voltage of 1.2 V or 1.4 V, selectable via the vcmsel bit in Register 15.

Gain Control

Gain control is distributed throughout the receive signal chain as shown in Figure 39. The RF front end contains 30 dB of control range: 18 dB in the LNA and 12 dB in the mixer transconductance stage. The two baseband active filter stages each provide 18 dB of gain control range in 6 dB steps. Filter characteristics (ripple and group delay) are best conserved if the active filter stages have equal gain. This results in a total of 36 dB gain control in 4× 12 dB steps for the filter stage. The variable gain amplifier (VGA) implements 24 dB of gain controllable in 1 dB steps. The base gain of the mixer is 18 dB, and the base gain of the VGA is −6 dB. This gives a total of 102 dB gain with 90 dB of gain control range.

The base gain of the mixer stage is 18 dB in WCDMA mode and 27 dB in GSM mode.

Table 6. Receive Gain Control in WCDMA mode

Stage	Gain Control	Control Steps
LNA	0 dB to +18 dB	3 × 6 dB steps
Mixer	+18 dB to +30 dB (WCDMA) +27 dB to +39 dB (GSM)	2 × 6 dB steps
Filter	0 dB to +36 dB	3 × 12 dB steps
VGA	−6 dB to +18 dB	24 × 1 dB steps

To simplify programming and to ensure optimum receiver performance and dynamic range, the user simply programs the total desired receive gain in dB via the rx_gain[6:0] bits in Register 11. The ADF4602 then decodes the gain setting and automatically distributes the gain between the various blocks. To allow some flexibility, predefined user inputs control the gain threshold points at which the LNA and mixer gain steps occur.

Bit settings mixstep[3:0] and lnastep[3:0] control the mixer and LNA gain threshold steps, respectively. An Excel spreadsheet detailing the receive gain decode system is available from Analog Devices, Inc., on request. Figure 38 shows an example gain distribution profile.

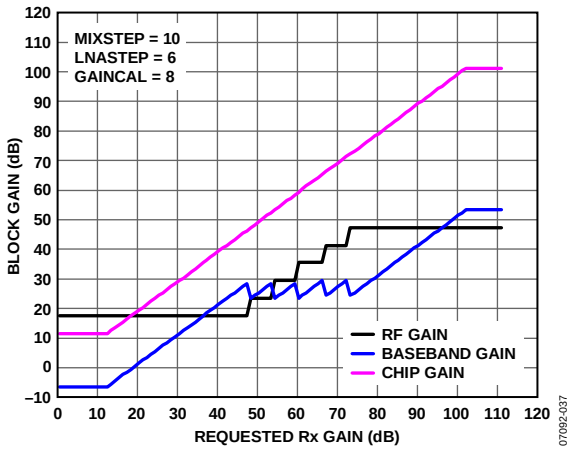

Figure 38. Gain Distribution Between RF and Baseband Blocks for Default Setting

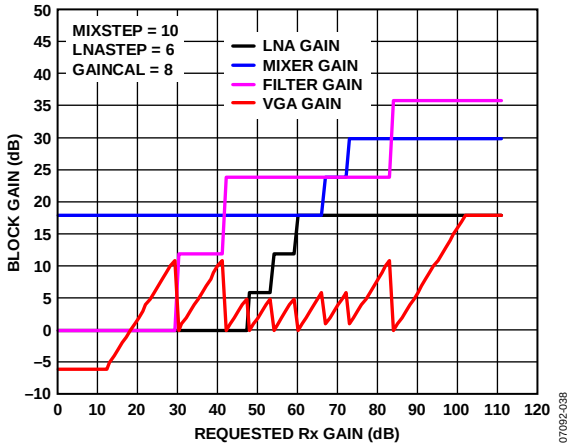

Figure 39. More Detailed Gain Distribution Profile

In addition, a gain calibration setting in Register 15 (gaincal[4:0]) is used to account for losses in the RF front end.

The total gain in the ADF4602 is given by

$$ReceiveGain = rxgain[6:0] - gaincal[4:0] + X \quad (2)$$

where X = 8 in WCDMA filter mode, and X = 17 in GSM filter mode. Rxgain[6:0] is the receive gain programmed in Register 11. Gaincal[4:0] is the gain calibration setting in Register 15, and is calculated using the following formula:

$$gaincal[4:0] = 8 - front\_end\_losses \quad (3)$$

where front_end_losses is the loss in the receive path due to duplexers/switches. This is useful for referencing the programmed gain to the antenna and accounting for any losses in the path.

For example, if the total receive front-end loss is 2 dB, the user should program gaincal[4:0] to 6 dB. If the user then requestes 80 dB of gain by programming rxgain[6:0] to 80 dB, the ADF4602 uses Equation 4 to give

$$ReceiveGain = 80 - 6 + 8 = 82 \text{ dB} \quad (4)$$

82 dB is the receive gain used internally by the ADF4602.

DC Offset Compensation

Due to the very high proportion of the total system gain assigned to the analog baseband function, compensating for dc offsets is an inherent part of any direct conversion solution. DC offsets are characterized as falling into two categories: static or slow varying and time varying

The ADF4602 architecture has been designed to reduce the amount of time varying dc offsets. The device also includes a dc offset control system. The control system consists of ADCs at the baseband output to digitize dc offsets: a digital signal processing block where the characteristics of the loop are programmed for customization of the loops transfer function, and trim DACs that are used to introduce the error term back into the signal path. The offset control transfer function can either be programmed to act as a servo loop that is automatically triggered by a gain change or as a high-pass filter (HPF) with an automatic fast settling mode that is also triggered by a gain change. Parameters of the servo loop, high-pass filter, and fast settling mode are set by the initial ADF4602 programming. In operation, the dc offset control system is fully automatic and does not require any external programming. Recommended default programming conditions for the dc offset compensation loop are shown in the Register Description section.

POWER MANAGEMENT

The ADF4602 contains integrated power management requiring two external power supplies: 3.3 V VDD and 1.8 V VINT. Figure 40 shows a block diagram.

VDD supplies the five integrated low drop-out regulators (LDOs), VSUP1 to VSUP5, that are used to supply the vast majority of the internal circuitry. VSUP6, VSUP7, and VSUP8 supply the receive PLL, transmit PLL, and reference block, respectively. These nodes require external connections to ensure good supply isolation and ensure a minimum level of interference between the PLL/reference blocks and the rest of the transceiver. VSUP6 and VSUP7 should be connected to VSUP3, whereas VSUP8 should be connected to VSUP2.

Each node, VSUP1 to VSUP8, should be externally decoupled to ground with a 0.1 µF capacitor. Y5V capacitors are not recommended for use here. X7R, X5R, C0G, or a similar type of capacitor should be used.

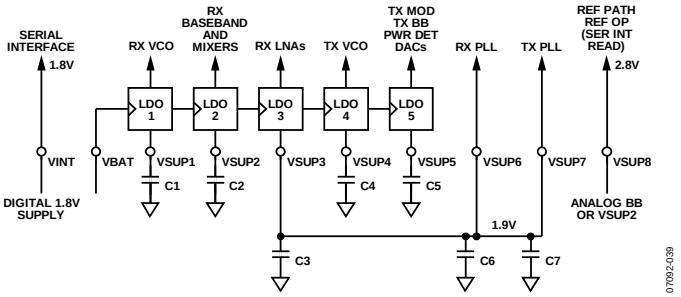

Figure 40. Power Management Block

VINT supplies the serial interface enabling register data preservation with minimum current consumption during power-down. This should be supplied with 1.8 V externally.

The five LDOs are individually powered up/down via bits ldoen[4:0] in Register 1. Table 7 summarizes the supply strategy.

Note that the reference path (VSUP8) supply is supplied from an external source or the internal VSUP2. The external supply option may be convenient so that the entire reference path can be shut down by collapsing a single supply.

VSUP8 can also be programmed to supply the voltage used for serial interface readback. See the Serial Port Interface (SPI) section for more information.

Table 7. Power Management Strategy

Pin	Connection	Usage	Volts
VINT	External	Serial interface control logic	1.8 V
VDD	External	Main device supply, DAC1	3.3 V
VSUP1	Internal LDO1	Receive VCO	2.6 V
VSUP2	Internal LDO2	Receive baseband and down-converter	2.8 V
VSUP3	Internal LDO3	Receive LNAs	1.9 V
VSUP4	Internal LDO4	Transmit VCO	2.6 V
VSUP5	Internal LDO5	Transmit baseband, modulator, DAC2, and GPOs	2.8 V
VSUP6	Connect to VSUP3	Receive synthesizer	1.9 V
VSUP7	Connect to VSUP3	Transmit synthesizer	1.9 V
VSUP8	VSUP2 or external	Reference path, reference buffer outputs; Optional: serial interface readback	2.8 V

FREQUENCY SYNTHESIS

The ADF4602 contains two fully integrated programmable frequency synthesizers for generation of transmit and receive local oscillator (LO) signals. The design uses a fractional-N architecture for low noise and fast lock-time. The fractional-N functionality is implemented with a third order Σ-Δ modulator. Figure 41 shows a block diagram of the synthesizer architecture.

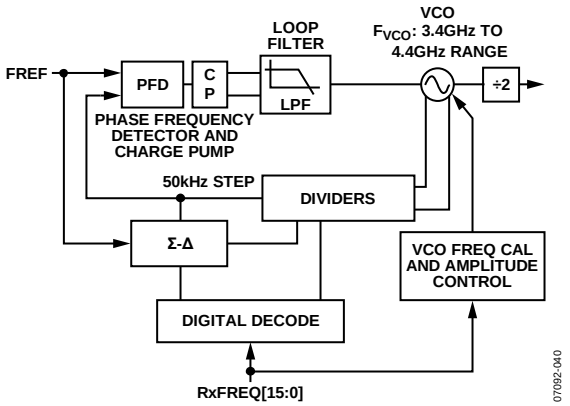

Figure 41. Frequency Synthesizer Block Diagram

All necessary components are fully integrated for both transmit and receive synthesizers, including loop filters, VCOs, and tank components. The VCOs run at 2× the high band frequency and 4× the low band frequency. The dividers are external to the synthesizer loop. This minimizes VCO leakage power at the desired frequency and tuning range requirements of the VCO. The VCOs use a multiband structure to cover the wide frequency range required.

The design incorporates both frequency and amplitude calibration to ensure that the oscillator is always operating with its optimum performance. The calibrations occur during the 200 µs PLL lock time and are fully self contained, requiring no user inputs.

The charge pump and loop filter are internally trimmed to remove variations associated with manufacture and frequency. This process is fully automated.

To aid simplified programming, the ADF4602 contains a frequency decode table for the synthesizers, meaning the programmer is not concerned with the internal operation of the counters and fractional-N system. Frequency step sizes of 50 kHz are possible with both transmit and receive synthesizers. The programming words rxfreq[15:0] and txfreq[15:0] set the frequency in 50 kHz steps from 0 MHz to 3276.75 MHz. Note that the synthesizers do not cover this full range. The frequency range for each synthesizer in high and low bands is given in the Specifications section.

When the high band is enabled, the programmed frequency is equal to the LO frequency. For low band operation, the programmed frequency should be set to 2× the desired LO frequency.

The transmit and receive synthesizers are enabled by setting Bit txsynthen and Bit rxsynthen in Register 1, respectively.

Reference Path

The ADF4602 requires a 26 MHz reference frequency input. A VCTCXO is used to provide this. The reference input is ac-coupled internally, so external ac coupling is not necessary.

The 26 MHz reference is internally buffered and distributed to the respective blocks, such as the synthesizer PFD inputs. Figure 42 shows a block diagram.

The ADF4602 provides two buffered outputs: a buffered version of the 26 MHz reference on Pin REFCLK and a 19.2 MHz WCDMA chip clock on Pin CHIPCLK. The 19.2 MHz chip clock is a multiple of the 3.84 MHz chip rate used in WCDMA. Thus, it can be used to clock ADCs/DACs elsewhere in the system. The chip clock is generated by an integrated PLL and contains no user settings.

Both outputs are slew rate limited and produce low swing digital outputs. The buffers contain their own 1.5 V regulator circuits to improve isolation and minimize unwanted supply noise. The 26 MHz and 19.2 MHz buffer outputs are enabled or disabled by programming Bit refclken and Bit chipclken (Register 1).

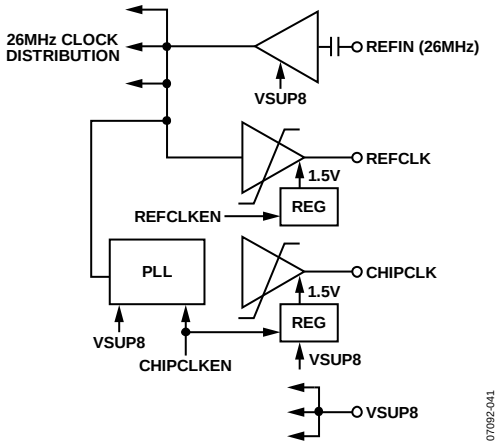

Figure 42. Reference Path Block Diagram

All reference sections are powered from VSUP8, which can safely be removed from the chip in isolation, to enter a low current power-down mode. Calibration data is not lost, but the reference frequency ceases to exist. As soon as VSUP8 is re-applied, oscillation begins. This is visible at the buffer outputs, as long as they were previously enabled.

SERIAL PORT INTERFACE (SPI)

The ADF4602 contains internal registers that are used to configure the device. The three-wire serial port interface provides read and write access to the internal registers. For write, read requests, and read operations, 26-bit transfers are used. The MSB of all words are transferred first.

Format

Figure 43 shows the format of the register write. This consists of a 5-bit address and 16-bit data words. The exception is register A1 = 00000, where the lower data byte is used as an 8-bit sub-address. In total, this creates 31 16-bit registers and 256 8-bit registers. The 31 16 bit registers are referred to in the text as "Register 31" for example, while the 256 8-bit sub registers are referred to as "Register 0.144".

OP is a 2-bit code specifying the type of operation being performed (see Table 8 for more information). The chip select code, CS, is a 3-bit field indicating which device on the bus is being programmed. For the ADF4602, CS should be set to 001 (D2, D1, D0).

Table 8. SPI Operation Code

OP[1]	OP[0]	Operation	Description
0	0	Write	Normal register write.
0	1	Set	Register bits corresponding to 1s in the data word are set. Other bits are not modified.
1	0	Clear	Register bits corresponding to 1s in the data word are cleared. Other bits are not modified.
1	1	Read	Register read request.

The read request format has the same address structure as the write format but does not contain a data field. Padding is used to maintain the 26-bit word length.

The readback format is the same as the word format during a write. Again, padding is used to maintain the 26-bit word length.

Table 9. SPI Chip Select Code

CS[2]	CS[1]	CS[0]	Device
0	0	1	ADF4602
All other permutations			Reserved

OPERATION AND TIMING

SCLK, SDATA, and SEN are used to transfer data into the ADF4602 registers. Data is clocked into the register, MSB, first on the rising edge of each SCLK. The data is transferred to the selected register address on the rising edge of SEN. See Figure 2 and Figure 3 for timing information.

Read

Figure 3 shows a read operation. First, a read request is written by the host to the ADF4602. SEN must remain high for at least three SCLK periods between the read request operation and the following read operation. The host must release the SDATA line during this period. The ADF4602 takes control of SDATA, and the read operation commences when the host device drives SEN low.

The SDATA output voltage during readback is set to 1.8 V or 2.8 V. Bit sif_vsup8 (Register 2) controls this. A 0 in this bit configures the device to use the 1.8 V VINT supply, whereas a 1 configures the 2.8 V VSUP8 supply. After power-up or after a soft reset, the ADF4602 defaults to 2.8 V readback mode.

OPERATION	BIT POSITION																									
	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRITE REGISTER 1 TO 31 W[25:0]	DATA D[15:0]																ADDRESS A1[4:0]					OP [1:0]		CS [2:0]		
WRITE REGISTER 0 W[25:0]	DATA D[7:0]								SUBADDRESS A2[7:0]								ADDRESS A1 = 00000					OP [1:0]		CS [2:0]		
READ REQUEST REGISTER 1 TO 31 Q[25:0]	RANDOM PADDING P[15:0]																ADDRESS A1[4:0]					OP [1:0]		CS [2:0]		
READ REQUEST REGISTER 0 Q[25:0]	RANDOM PADDING P[7:0]								SUBADDRESS A2[7:0]								ADDRESS A1[4:0]					OP [1:0]		CS [2:0]		
READ REGISTER 1 TO 31 Q[25:0]	DATA D[15:0]																ADDRESS A1[4:0]					OP = 11		CS [2:0]		
READ REGISTER 0 Q[25:0]	DATA D[7:0]								SUBADDRESS A2[7:0]								ADDRESS A1 = 00000					OP = 11		CS [2:0]		

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Figure 43. SPI Register Write Format

REGISTERS

REGISTER MAP

GENERAL USER REGISTERS

A1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT[1]	R/W
1			rxen	refclk en	chipclk en	ldoen[4:0]					txen	txbs	txsynth en	rxbs[1:0]		rxsynth en	0x2FFD	W
2															sif_ vsup8	reset_ soft	0x0002	W

RECEIVER USER REGISTERS

A1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT[1]	R/W
10	rxfreq[15:0]																0x9858	W
11										rxgain[6:0]							0x0000	W
12	rfskip[3:0]				sdmen[3:0]				mixstep[3:0]				lnastep[3:0]				0x0FA6	W
13	osadc2x[3:0]				nper2[3:0]				nper1[3:0]				nper0[3:0]				0x103E	W
14	nint3[3:0]				nint2[3:0]				nint1[3:0]				nint0[3:0]				0xEE53	W
15					vcmsel	swapq	swapi	rxbw[2:0]			gaincal[4:0]					sdmosr	0x0890	W

TRANSMITTER USER REGISTERS

A1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT[1]	R/W
21				test_I/swap_I		test_Q/swap_Q		gain_blanksel [1:0]		cmmod	vcm_sat_thres[5:0]						0x001F	W
22	dacgpo _owen	gpo_ow[3:0]				padac2_ow[5:0]						padac1[4:0]					0x8000	W
26	txfreq[15:0]																0x0000	W
28	txpwr_set[11:0]															cntrl_ mode	0x0001	W
31												nvmld					0x0000	W

SUB-ADDRESS REGISTERS

A1	A2	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT[1]	R/W
0	144						reserved[1:0]			0x06	W
0	151	vsup2[7:0]								0x6F	W
0	153	reserved[7:0]								0x85	W
0	155	reserved[7:0]								0x78	W
0	165	reserved[7:0]								0x20	W
0	170	en_mix[3:0]								0xF0	W
0	171						buffstate			0x04[2]	W
0	174	buff_value[7:0]								0x5F[3]	W
0	175	reserved[7:0]								0x14	W

NOTES
[1]THESE ARE RECOMMENDED DEFAULT SETTINGS THAT SHOULD BE PROGRAMMED INTO THE REGISTERS.
[2]DEFAULT SHOWN IS FOR BAND 1 OPERATION. SET TO 0x00 IF TRANSMIT FREQUENCY < 21100MHz.
3DEFAULT SHOWN IS FOR BAND 1 OPERATION. SET TO 0x50 IF TRANSMIT FREQUENCY < 21100MHz.

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Figure 44. Register Map

REGISTER DESCRIPTION

Table 10. General User Registers

Register	Bit	Bit Name	Description	
1, A1	13	rxen	Set this bit high to enable the receiver. A low here disables the receiver.	
	12	refclken	Setting this bit high enables the 26 MHz reference output buffer.	
	11	chipclken	Setting this bit high enables the19.2 MHz chip clock output buffer.	
	[10:6]	ldoen	The on-chip LDOs are powered down individually. For normal operation all LDOs should be enabled (Bits[10 : 6] = [11111])	
			ldoen[10:6][1]	**Mode**
			XXXX1	VSUP1 2.6 V enable
			XXX1X	VSUP2 2.8 V enable
			XX1XX	VSUP3 1.8 V enable
			X1XXX	VSUP4 2.6 V enable
			1XXXX	VSUP5 2.8 V enable
	5	txen	Setting this bit high enables the transmitter.	
	4	txbs	This bit controls which of the transmit outputs is in use. 0 = low band (TXLBRF), 1 = high band (TXHBRF).	
	3	txsynthen	Setting this bit high enables the transmit synthesizer.	
	[2:1]	rxbs	These bits control the receiver band select.	
			rxbs[2:1]	**Operation**
			00	Reserved
			01	Low band enable (RXLB)
			10	High Band 1 enable (RXHB1) (default)
			11	High Band 2 enable (RXHB2)
	0	rxsynthen	Setting this bit high enables the receive synthesizer	
2, A1	1	sif_vsup8	The serial port readback (SDATA) output voltage is changed from 1.8 V to 2.8 V with this bit. 0 = use 1.8 V VINT supply, 1 = use 2.8 V VSUP8 supply. After power-up or after a soft reset, the ADF4602 defaults to 2.8 V readback mode.	
	0	reset_soft	A rising edge on this bit starts a 50 µs reset pulse for the full chip. This bit is self clearing. It is recommended that a soft reset be performed after power-up.	

[1] X = don't care.

Table 11. Receiver User Registers

Register	Bit	Bit Name	Description
10, A1	[15:0]	rxfreq	These bits set the receive synthesizer frequency in 50 kHz steps from 0 MHz to 3276.75 MHz. For the high bands this is equal to the channel frequency, and for the low bands it is 2× the channel frequency. For example:
			Bit 15 to Bit 0 (Hex) / **HB1, HB2 Synthesizer Frequency** / **LB Synthesizer Frequency** 0x9470 / 1900 MHz / 950 MHz 0x9858 / 1950 MHz / 975 MHz
11, A1	[6:0]	rxgain	These bits set the receiver gain in conjunction with the gaincal[4:0] setting in register 15. LSB = 1 dB. 0x00 = 0dB, 0x7F = 127 dB. *Gain = rxgain − gaincal + X* where *X* is 8 in WCDMA mode and 17 in GSM mode. The mode is selected by the rxbw bits in Register 15. With mixstep = 6 and lnastep = 10, the valid range for rxgain is from 12 dB to 102 dB. Settings outside of these are clipped at 12 dB and 102 dB. See Figure 38 for an example.
12, A1	[15:12]	rfskip	Skip offset control state when no RF gain step occurred for State 3 to State 0. Default = 0x0 = 0.
	[11:8]	sdmen	Σ-Δ modulator enable for State 3 to State 0. Default = 0xF = 15.
	[7:4]	mixstep	Gain decode threshold for mixer gain reduction step. LSB = 4 dB steps. Default = 0xA = 10.
	[3:0]	lnastep	Gain decode threshold for LNA gain reduction step. LSB = 4 dB steps. Default = 0x6 = 6.
13, A1	[15:12]	osadc2x	Offset measurement ADC range for State 3 to State 0. Default = 0x1 = 1.
	[11:8]	nper2	State duration for State 2. Default = 0x0 = 0.
	[7:4]	nper1	State duration for State 1. Default = 0x3 = 3.
	[3:0]	nper0	State duration for State 0. Default = 0xE = 14.
14, A1	[15:12]	nint3	Integrator time constant for State 3. Default = 0xE = 14.
	[11:8]	nint2	Integrator time constant for State 2. Default =0xE = 14.
	[7:4]	nint1	Integrator time constant for State 1. Default = 0x5 = 5.
	[3:0]	nint0	Integrator time constant for State 0. Default = 0x3 =3.
15, A1	11	vcmsel	This sets the receive baseband output common-mode voltage. 0 = 1.2 V, 1 = 1.4 V.
	10	swapq	Setting this bit high swaps the differential Q outputs, RXBBQ and RXBBQB.
	9	swapi	Setting this bit high swaps the differential I outputs, RXBBI and RXBBIB.
	[8:6]	rxbw	This bit controls the receive baseband filter bandwidth.
			rxbw [8:6] / **Filter Mode** 000 / Fifth order WCDMA filter (not recommended for femtocells) 010 / Seventh order WCDMA filter (recommended WCDMA filter for femtocells) 111 / GSM filter Else / Reserved
	[5:1]	gaincal	These bits are used for calibration of front-end loss. LSB = 1 dB, 0x00 = 0 dB, 0x1F = 31 dB. It is used in the calculation of the receive gain. See rxgain in Register 11. If not used for calibration, this should be set to 8 in WCDMA mode and 17 in GSM mode.
	0	sdmosr	Offset loop Σ-Δ modulator over sampling ratio. 1 = 4×, 0 = 2× (default)

Table 12. Transmitter User Registers

Register	Bit	Bit Name	Description		
21, A1	[12:11]	test_I/swap_I	These bits allow various options on the I inputs as detailed in the following table:		
			Bits	**Function**	
			00	Normal operation	
			01	Swap I differential inputs for ease of PCB routing to DAC	
			10	Zero input on I inputs	
			11	DC offset applied to I inputs; creates large carrier at RF	
	[10:9]	test_Q/swap_Q	These bits allow various options on the Q inputs as detailed in the table below:		
			Bits	**Function**	
			00	Normal operation	
			01	Swap Q differential inputs for ease of PCB routing to DAC	
			10	Zero input on Q inputs	
			11	DC offset applied to Q inputs: creates large carrier at RF	
	[8:7]	gain_blanksel	During a transmit gain change, some spectral splatter may occur at the output of the transmitter. These bits allow the input baseband signal at the input to the low-pass filter to be blanked for a short period, to reduce the spectral splatter observed during the gain change.		
			gain_blanksel[8:7]	**Operation**	
			00	Default setting; no blanking	
			01	230 ns blanking	
			10	540 ns blanking	
			11	850 ns blanking	
	6	cmmod	This bit adjusts the internal modulator common-mode setting. It should be set to 0. Setting this bit to 1 results in reduced power consumption but degrades transmit linearity.		
	[5:0]	vcm_sat_thres	This bit should be set to 0x1F for normal operation.		
22, A1	15:	dacgpo_owen	Setting this bit high allows the user to have manual control over DAC2 and GPO1 to GPO4.		
	[14:11]	gpo_ow	These bits allow manual control of GPO 1 to GPO 4. Bit dacgpo_owen must be set to 1 to allow this mode of operation. Each bit controls one of the GPOs as per the following table. This allows all possible permutations of GPO output combinations.		
			gpo_ow[14 :11][1]	**Mode**	
			XXX1	GPO1 high	
			XX1X	GPO2 high	
			X1XX	GPO3 high	
			1XXX	GPO4 high	
	[10:5]	padac2_ow	These bits allow manual control of DAC2. Bit dacgpo_owen must be set to 1 to allow this mode of operation.		
	[4:0]	padac1	These bits control DAC1.		
26, A1 Write	[15:0]	txfreq	These bits set the transmitter synthesizer frequency in 50 kHz steps from 0 MHz to 3276.75 MHz. For the high bands, this is equal to the channel frequency, and for the low bands it is 2× the channel frequency. For example:		
			Bit 15 to Bit 0 (Hex)	**HB Synthesizer Frequency**	**LB synthesizer Frequency**
			0xA730	2140 MHz	1070 MHz
			0xA988	2170 MHz	1085 MHz

Register	Bit	Bit Name	Description
28, A1 Write	[15:4]	txpwr_set	Requested transmit power at antenna. LSB = 1/32 dBm, 0x000 = −80 dBm, 0xFFF = 47.96875 dBm. The output power is referenced to a full scale sine wave applied to the transmit baseband inputs. For WCDMA modulated signals, the output power measured in a 3.84 MHz bandwidth is reduced by the peak to average ratio of the signal. See the I/Q Modulator section for more details. The valid range of transmit output power setting is −80 dBm to +10 dBm. Output clipping may occur sooner, depending on the PAR of the applied signal. The txpwr_set register should be updated periodically, or with every 5°C change in temperature to ensure accurate output power. See the VCO Output section for more details.
	0		Set this bit to 1 to control the output power from the txpwr_set bits.
31, A1 Write	4	nvmld	Setting this bit to 1 triggers a manual load of the nonvolatile memory contents. See the Software Initialization Procedure section for more details.

[1] X = don't care.

Table 13. Sub-Address Registers

Register	Bit	Bit Name	Description
0.144, A2 Write	[2:1]	reserved[1:0]	These bits should be set to 11 for normal operation.
0.151, A2 Write	[7:0]	vsup2[7:0]	These bits control the VSUP2 regulator voltage and should be set to 0x6F for normal operation. During the initialization sequence, the VSUP2 voltage is temporarily set to 3.1 V. See the Software Initialization Procedure section for more details.
0.153, A2 Write	[7:0]	reserved[7:0]	These bits should be set to 0x85 for normal operation.
0.155, A2 Write	[7:0]	reserved[7:0]	These bits should be set to 0x78 for normal operation.
0.165, A2 Write	[7:0]	reserved[7:0]	These bits should be set to 0x20 for normal operation.
0.170, A2 Write	[7:4]	en_mix[3:0]	These bits enable the I, IB, Q, and QB channels of the modulator separately. Set these bits to all 1s to enable the modulator for normal operation.
0.171, A2 Write	2	buffstate	This bit controls the transmit VCO buffer state. For transmit synthesizer frequencies > 2100 MHz (Band 1) the buffer state should be set to 1, and the corresponding VCO buffer value in R0.174 should be set to 0x5F. This ensures correct device operation for frequencies > 2100 MHz. For operation below 2100 MHz (Band 2). the buffer state should be set to 0, and the corresponding VCO buffer value in R0.174 should be set to 0x50. This ensures correct device operation for frequencies < 2100 MHz.
0.174, A2 Write	[7:0]	buff_value[7:0]	These bits should be set to 0x5F for transmit frequencies >2100 MHz, and 0x50 for transmit frequencies <2100 MHz. See the description for Register 0.171 for more.
0.175, A2 Write	[7:0]	reserved[7:0]	These bits should be set to 0x14 for normal operation.

SOFTWARE INITIALIZATION PROCEDURE

INITIALIZATION SEQUENCE

Table 14 shows the initialization sequence that should be used after power-up. Note that the 26 MHz reference clock must be applied to the REFIN pin before programming begins. The default settings are described in the comments section, and some settings, such as output frequency, gain, and GPO settings, may vary from those required in the end application of the user. The user can substitute his own settings in these instances.

Table 14. Initialization Sequence

Step	Register[1]	Data	Comment
1	02	0x0003	Performs a soft reset of the ADF4602. The reset takes 50 µs, and no registers should be written to during this period. After 50 µs, programming can continue as normal. This bit is self clearing. If using 1.8 V logic levels, this register should be programmed to 0x0001 instead of 0x0003.
2	0.151	0xE0	Set VSUP2 to 3.1 V. See the Nonvolatile Memory (NVM) Initialization section for more details.
3	31	0x0010	Transfers non-volatile memory (NVM) contents to registers. Wait 200 µs before next programming step.
4	31	0x0000	Negate bit set in last programming step.
5	0.151	0x6F	Set VSUP2 back to 2.8 V.
6	01	0x2FDD	Enables receiver and disables transmit output. Selects TXHBRF pin as the transmit output and RXHB1 as the receive input. Enables all on-chip regulators. 19.2 MHz output clock is enabled, 26 MHz output clock is disabled. If it is desired to disable the 19.2 MHz output clock, this register is programmed to 0x27DD.
7	12	0x0FA6	Default settings for mixer and LNA gain reduction steps.
8	13	0x103E	Default settings.
9	14	0xEE53	Default settings.
10	15	0x0890	Sets received gain calibration, WCDMA filter mode, and output common-mode voltage to 1.4 V.
11	21	0x001F	Default settings.
12	22	0x8000	Enables DAC and GPO manual control.
13	0.144	0x06	Default settings.
14	0.155	0x78	Default settings.
15	0.153	0x85	Default settings.
16	0.165	0x20	Default settings.
17	0.170	0xF0	Default settings.
18	0.171	0x04	If transmit synthesizer frequency is >2100 MHz
		0x00	If transmit synthesizer frequency is <2100 MHz
19	0.174	0x5F	If transmit synthesizer frequency is >2100 MHz
		0x50	If transmit synthesizer frequency is <2100 MHz
20	0.175	0x14	Default settings.
21	11	0x0050	Receiver gain set to 80 dB.
22	10	0x9858	Receiver synthesizer frequency set to 1950 MHz. The PLL takes 200 µs to lock. Registers should not be written to during this period.
23	26	0xA730	Transmit synthesizer frequency set to 2140 MHz. The PLL takes 200 µs to lock. Registers should not be written to during this period.
24	01	0x2FFD	Enables transmit output.
25	28	0xA001	Enables control of the output power and sets the txpwr_set field to 0 dBm. Control of output power is via the txpwr_set bits.

[1] Register numbers 0.xxx are 8-bit registers as described in the SPI Interface section of the ADF4602-x datasheet.

Nonvolatile Memory (NVM) Initialization

The ADF4602 has on-chip non-volatile memory (NVM) that contains chip factory calibration coefficients. A soft reset of the device transfers the contents of NVM to internal registers; however, this has been found to be unreliable if performed at temperatures below 0°C. The software work-around outlined in Step 2 to Step 5 of Table 14 ensures that the NVM data is transferred reliably under all operating conditions. It involves setting the VSUP2 on-chip regulator to 3.1 V, manually transferring the data by setting the nvmld bit in Register 31, and then resetting the VSUP2 regulator to 2.8 V. Device programming can then continue as normal.

Programming Transmit and Receive frequencies

After initialization, the transmit/receive synthesizer frequencies may need to be changed. To change the transmit frequency, write the new frequency word to Register 26. When a new transmit frequency is programmed, the transmit output power is automatically turned off to prevent any unwanted transmissions as the PLL locks. The user should wait 200 µs (time taken for PLL to lock), and then set the output power to the desired value by writing to Register 28.

If the user disables the transmit synthesizer, the transmit output power must be turned off before reenabling the transmit synthesizer. This is achieved by two means: setting Bit D5 in Register 1 or setting the output power in Register 28 to a minimum.

After reenabling the synthesizer, and then locking the synthesizer to a frequency by programming the frequency word in Register 26, the user can reenable the output power.

To change the receive frequency, simply program the new frequency in Register 10, and wait 200 µs before using the device as a transceiver. The receive gain is set at any time (apart from during the 200 µs PLL locking transient).

APPLICATIONS INFORMATION

INTERFACING THE ADF4602 TO THE AD9863

The AD9863 mixed signal front-end processor is recommended for use with the ADF4602. The AD9863 contains dual 12-bit ADCs and dual 12-bit DACs for sampling the ADF4602 receive signal and providing the transmit baseband signal to the ADF4602. This section discusses the connections necessary between the devices.

Transmit Interface

The AD9863 TxDAC core provides dual, differential current output DACs generated from the 12-bit data. The full scale output current, $I_{OUTFSMAX}$, is set by means of an external resistor, R_{SET}. The relationship between $I_{OUTFSMAX}$ and R_{SET} is as follows:

$$I_{OUTFSMAX} = 67 \times \left(\frac{1.23\,V}{R_{SET}} \right)$$

Setting R_{SET} to 3.9 kΩ gives the optimal dynamic setting for the TxDACs and results in a full scale output current of 20 mA.

The ADF4602 transmit baseband inputs accept a 1.2 V common-mode input signal with 1 V p-p differential swing. The configuration in Figure 45 is used to provide this from the AD9863 TxDACs.

Resistor R_{DC} set up the dc common-mode voltage, whereas load Resistor R_L sets the differential swing. The differential swing, V_{DIFF}, is a function of the load resistor, R_L, and the DAC full scale current, $I_{OUTFSMAX}$, according to

$$V_{DIFF} = \frac{2 \times I_{OUTFSMAX} \times R_{DC} \times R_L}{2 \times R_{DC} + R_L} = f(I_{OUTFSMAX}) = g(R_L)$$

The common-mode voltage V_{CM} is set by

$$V_{CM} = \frac{I_{OUTFSMAX}}{2} \times R_{DC}$$

Using these equations, R_{DC} is set to 120 Ω to give 1.2 V common-mode voltage, and R_L is set to 63 Ω to give a 1 V p-p differential input swing.

The AD9863 transmit programmable gain amplifier (TxPGA) provides 20 dB of simultaneous gain range for both DACs and is controlled via the SPI port. The gain is in the range of 10% to 100% $I_{OUTFSMAX}$. Coarse gain controls are also available for each DAC output. Maximum settings (255) for both TxPGA gain and coarse gain controls (full gain) are recommended. This is because the DAC output common-mode voltage V_{CM} is designed with a specific $I_{OUTFSMAX}$. Varying the DAC gain results in a different $I_{OUTFSMAX}$ and consequently, a different V_{CM}, which is not optimum for the ADF4602. With the DAC gain set permanently at maximum, the transmit output power is controlled via the ADF4602 Tx power setting.

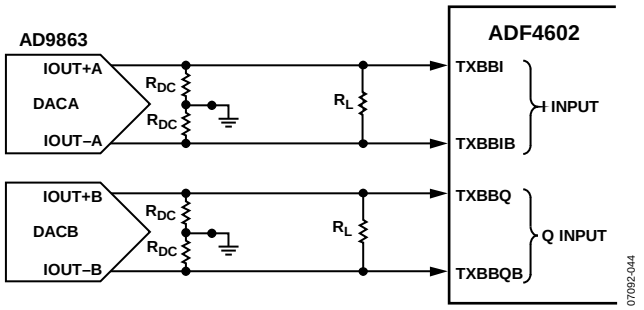

Figure 45. AD9863 TxDAC to ADF4602 Baseband Input Interface

Receive Interface

The AD9863 ADC input consists of a differential input resistance of 2 kΩ and a switched capacitor circuit with a 2 V p-p differential full scale input level. The input is self biased to mid-supply, or, alternatively, is programmed to accept an external dc bias. The ADF4602 receive baseband outputs can provide this external dc bias (1.4 V), and this is the preferred interface between the two devices. The vcmsel bit in Register 15 should be set to 1 to give the 1.4 V common-mode voltage from the ADF4602, and the AD9863 input bias should be disabled. A direct connection can then be made between the ADF4602 receive baseband outputs and the AD9863 ADC inputs.

The sampling action of the ADC sample and hold capacitor can introduce a kick-back effect onto the input signal. This can lead to spurs in the receive signal at integer multiples of the ADC sampling frequency. These spurs can degrade the sensitivity of the receiver on channels containing these spurs. To reduce these spurs and improve the sensitivity, filtering capacitors of 100 pF to ground should be placed on each receive baseband output. Figure 46 shows the interface between the two devices.

Receive Sensitivity

Figure 26 shows the ADF4602 receive sensitivity vs.frequency. The sensitivity degradation due to the 63rd and 64th harmonics of the 30.72 MHz ADC sampling frequency can be seen near 1935 MHz and 1966 MHz. The 100 pF filtering capacitors to ground were used at the ADC inputs for this plot. Note also the sensitivity degradation due to the 26 MHz reference frequency harmonics at 1924 MHz, 1950 MHz, and 1976 MHz. The degradation in sensitivity is less than 3 dB for these harmonics. Overall, the solution exceeds the 3GPP sensitivity specifications by 6 dB across the frequency range.

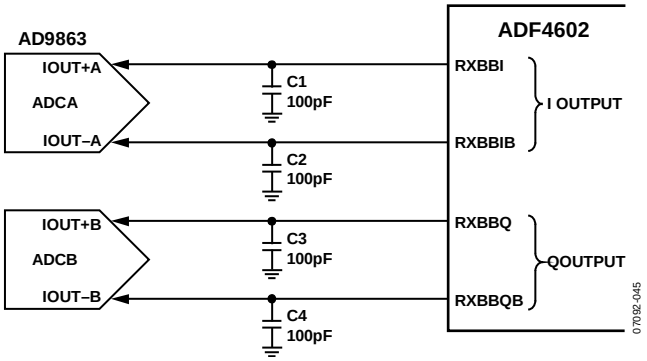

Figure 46. ADF4602 Receive Baseband Output to AD9863 ADC Interface

OUTLINE DIMENSIONS

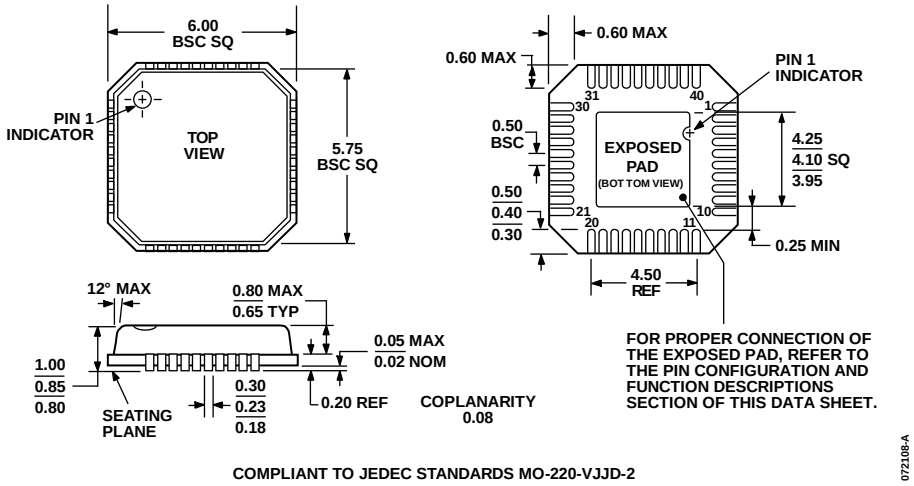

Figure 47. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4602BCPZ	0°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40-1
ADF4602BCPZ-RL	0°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40-1

[1] Z = RoHS Compliant Part.

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